SONY

Technical Training

WAX 2 CHASSIS

(AEP Models)

Jacek Wozniczko

CONTENTS

1. INTRODUCTION

1.1. Line up

KDL-26S2000 E/U
KDL-32S2000 E/U
KDL-40S2000 E/U
KDL-46S2000 E/U

KDL-26S2010 E/U
KDL-32S2010 E/U
KDL-40S2010 E/U
KDL-46S2010 E/U

KDL-26S2020 E/U
KDL-32S2020 E/U

HD ready **Definition**

- **Display minimum resolution of at least 720 lines in 16:9 format**
- **Supports both 720p and 1080i**
- **Contains both component (YUV) and HDMI/DVI (with HDCP)**

1.2. Main Features

- High Brightness, wide viewing angle (S-PVA) high resolution WXGA (1366 x 768)16:9 LCD panel. S-LCD Panels
- Television System Analog :B/G/H,L,I,D/K, Digital: DVB-T
- Color System: PAL/PAL 60/SECAM/NTSC 3.58 4.43(Video In)
- Highly integrated system - **on-a-chip**
- 3D Digital Comb Filter
- Integrated Digital TV Tuner (DVB-T)
- TXT level 1.5
- Teletext Page Memory 250 pages
- Smart Link
- OSD 18 languages
- HD Ready for High Definition era
- HDMI Input
- PC Input
- High Sound Quality - Digital Audio Amplifier, TruSurround XT, BBE Digital
- Compact and Slim Design
- Easy and Convenient Functions for Daily Use - On/Off Timer, Light Sensor
- VESA: compliant mounting holes

1.3. Video Specifications

- 1366 x 768 WXGA LCD Panel
- High Contrast (1300 : 1)
- High Brightness(500cd/m2)
- 3D Comb Filter
- Advanced Video Processor: Motion and edge adaptive I/P converter
- Advanced Video Processor: Contrast enhancer circuit
- Advanced Video Processor: MPEG noise reduction
- Advanced Video Processor: Green and blue enhancer
- 1080i Ready / Pal Progressive
- Wide Mode (Smart/Zoom/ 4:3/14:9/Wide)
- Picture Freeze

1.4. Audio Specifications

- Digital Audio Amplifier,
- TruSurround XT
- BBE Digital
- Audio out 10W +10W
- Sound Mode: Dynamic/Standard/Custom
- Audio Out (Fixed)

1.5. Panel Specification

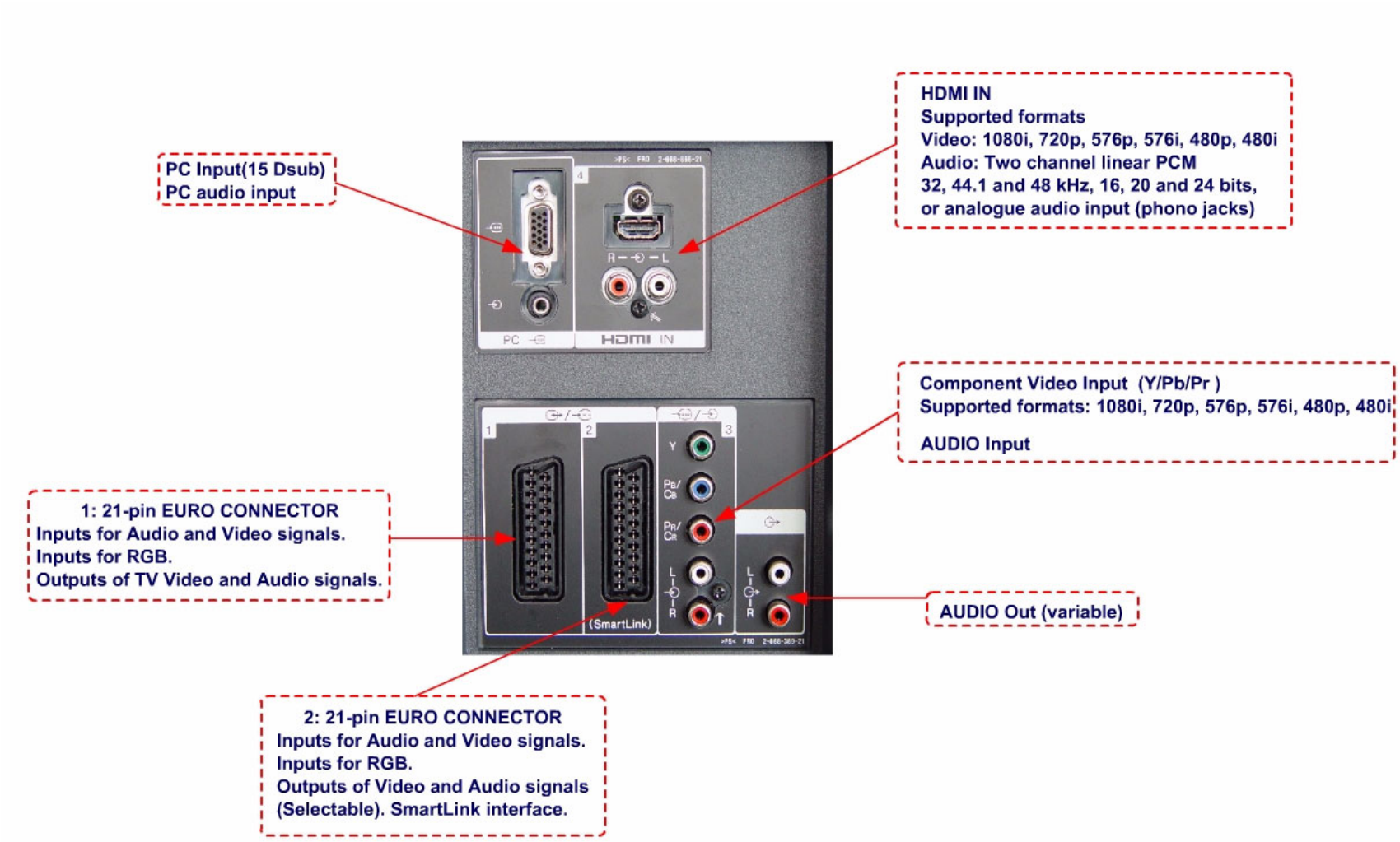
Panels used in WAX 2chassis are colour active matrix liquid crystal displays (LCD) that use amorphous silicon TFT (Thin Film Transistor) as switching components. Each model is composed of a TFT LCD panel, a driver circuit and a back light unit. These panels are intended to support applications to provide an excellent performance for Flat Panel Displays such as Home-alone Multimedia TFT-LCD
TVs, Display terminals for AV application products, and High Definition TV (HDTV).

1.6. Features

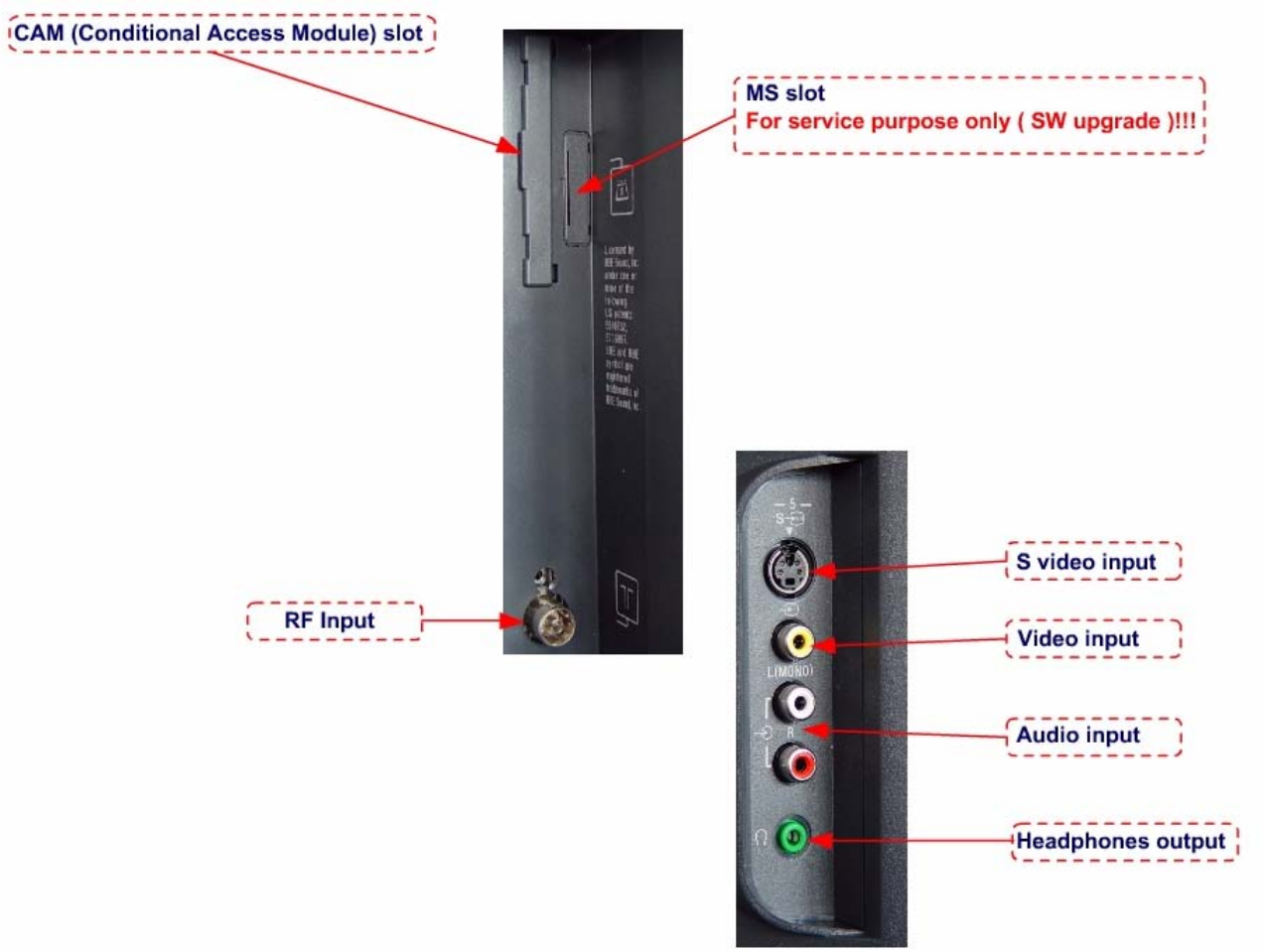
- High contrast ratio > 1000
- Brightness – 500 cd/m²
- SPVA (Super Patterned Vertical Align) mode
- Wide viewing angle (±89°)
- High speed response 8-12 ms G-to-G
- WXGA (1366 x 768 pixels) resolution (16:9)
- Display colours 8bit-16.7M
- Low Power consumption
- CCFTs (Cold Cathode Fluorescent Tube)
- DE(Data Enable) mode
- LVDS (Low Voltage Differential Signalling) interface (1pixel/clock)

1.7. Input/Output Terminals

Input/Output Terminals [REAR]



Input/Output Terminals [SIDE]

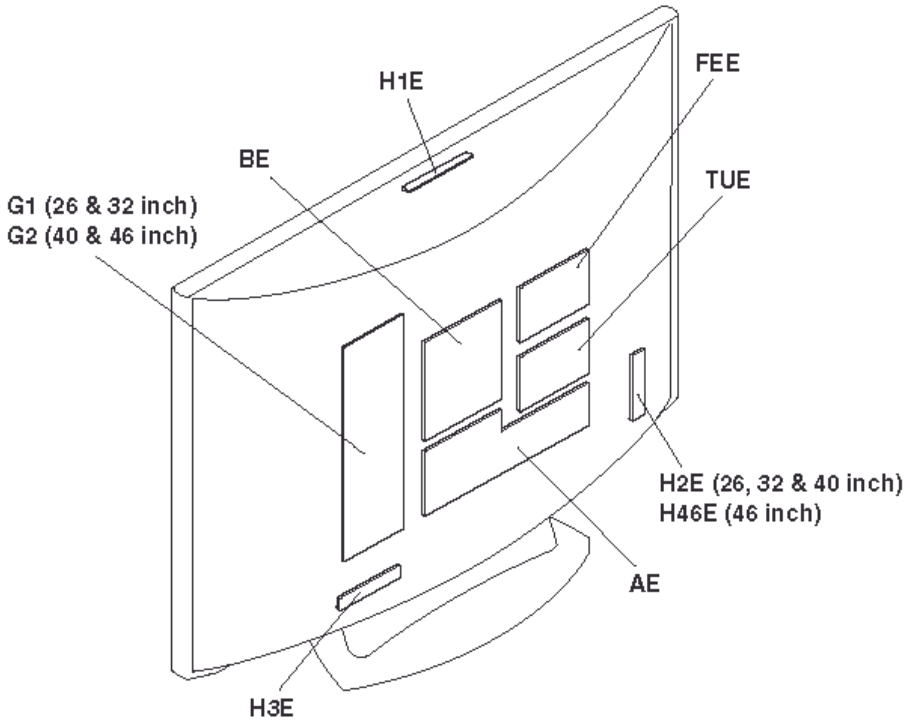


1.8. Remote Commander

New Remote Commander RM-ED005 for all WAX chassis models

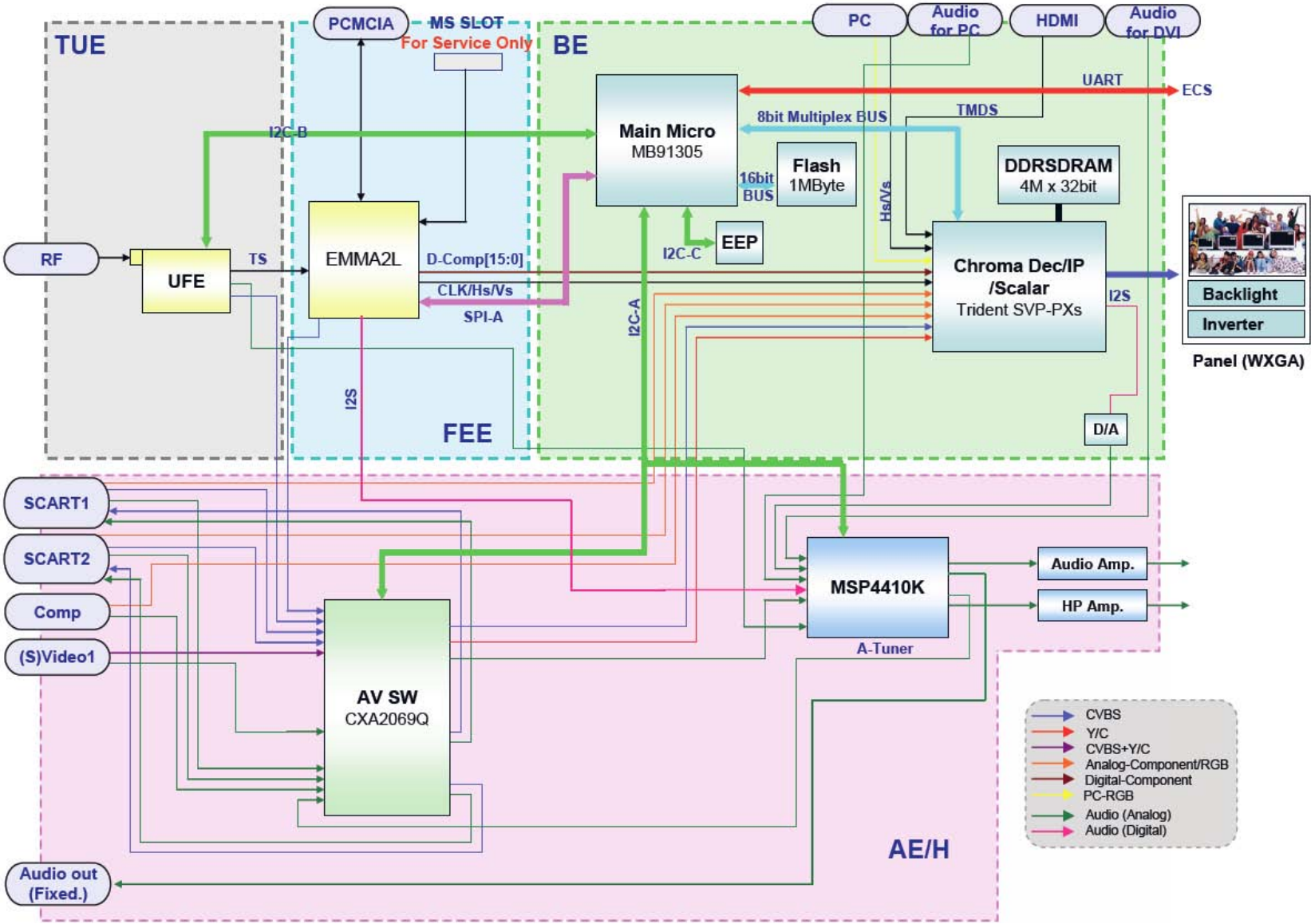
2. CHASSIS STRUCTURE AND BLOCK DIAGRAM

2.1. Chassis Structure and Board Function

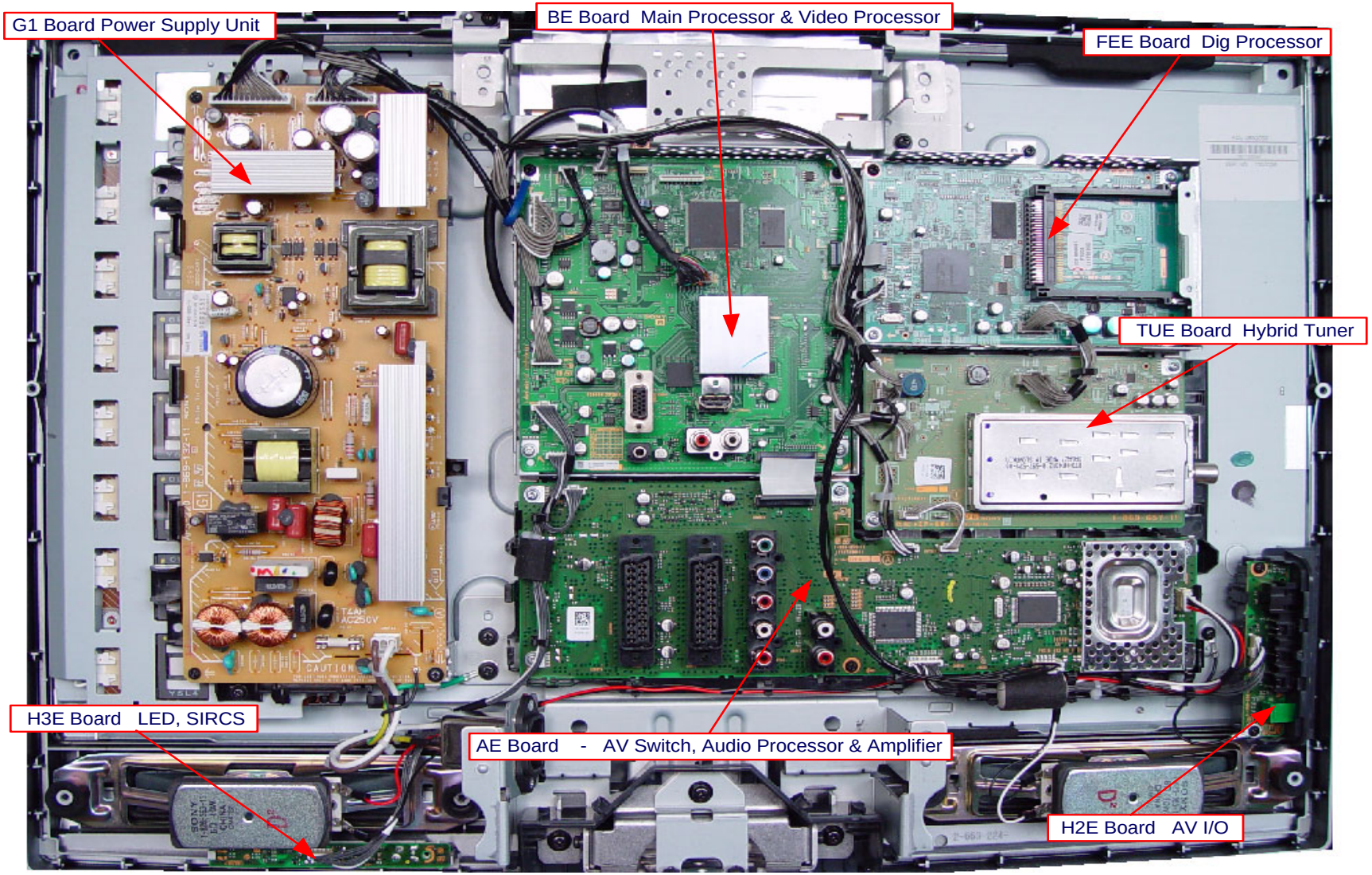


AE Board - AV Switch, Audio Processor & Amplifier
BE Board - Main Processor & Video Processor
FEE Board - Digital Microprocessor
G1 Board - Power Supply (26 & 32 inch)
G2 Board - Power Supply (40 & 46 inch)
H1E Board - Switch Panel
H2E Board - AV I/O (26,32,40 inch)
H3E Board - LED, SIRCS
H6E Board - AV I/O (46 inch)
TUE Board - Hybrid Tuner

2.2. Block Diagram



2.3. Boards Overview (KDL 26S200)



2. 4. Main device overview

Device	Board	Reference	Function
CXA2069Q	AE	IC2001	AV Switch
MSP4400K	AE	IC7001	Audio Processor
M61571AFP	AE	IC7007	Audio Power Amp
NJM4558V	AE	IC7601	Line_out Amp
NJM3414AV	AE	IC7602	HP Amp
MB91305	BE	IC1001	µPC
S29AL016D70	BE	IC1002	16Mbit FlashROM
LM393DT	BE	IC1003	AV Link Comparator
PST 3629UL	BE	IC1004	Reset
M24256-BWMN6T	BE	IC1005	EEPROM (NVM)
TMP75AIDR	BE	IC1007	Temp Sensor
SN74LV132APWR	BE	IC1008	Logic IC
S-35390A-J8T1	BE	IC1009	Port Exp
CXD9199CG	BE	IC5000	Trident SVP-PX
SN74CBTLV3245APWR	BE	IC5201/5202	CPU I/F
EM6A9320B1-5MGN	BE	IC5500	DDR_SDRAM 128Mbit
M24C02-WMN6T	BE	IC6000	PC EDID (NVM)
BR24L02F-WE2	BE	IC9001	HDMI IN EDID (NVM)
BD9775FV	BE	IC7000	DC-DC Conv
UPD61123F1-100-KA3-A	FEE	IC3100	EMMA2L Processor
EDD1216AATA-6B-E	FEE	IC3200	DDR SDRAM
K9F2808U0C-PCB0T	FEE	IC3206	Flash Memory
74LVC541APW	FEE	IC3301-3312	BUFFER & LINE DRIVER
FA5501AN	G1	IC6301	Active PFC Control
MIP2H2	G1	IC6104	STBY Switching Regularor
CXD9841M	G1	IC6501	Main Switching Regularor
FA5501AN	G2	IC6502	Active PFC Control
CXD9841M	G2	IC6100	Main Switching Regularor
MIP2H2	G2	IC6301	STBY Switching Regularor
BTD-HF431Z	TUE	TU3901	HYBRID Tuner

3. POWER SUPPLY

3.1. General info

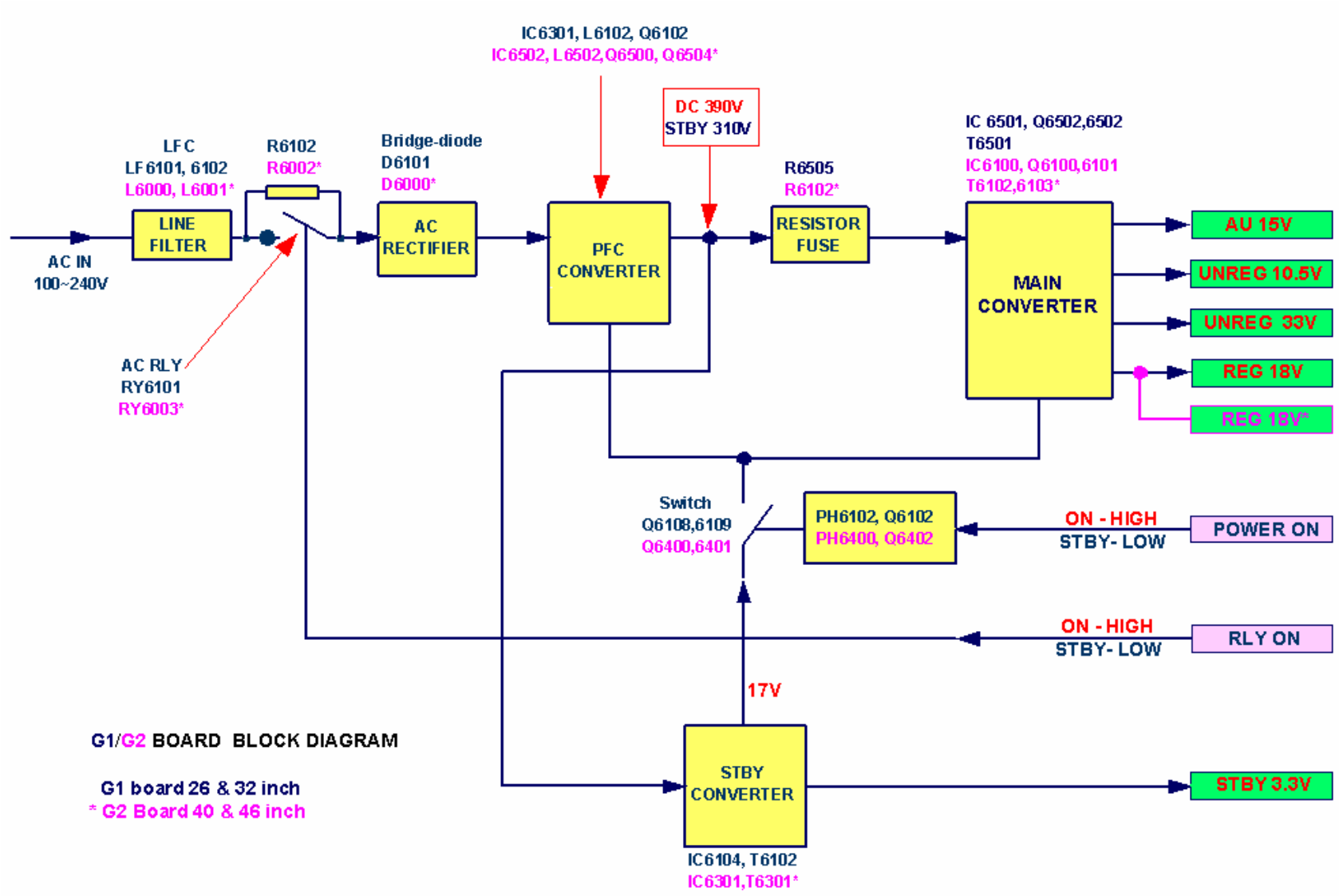
The power supply of the WAX2 chassis is located on the G1 or G2 board, it is designed to operate within an input voltage range from 100V to 240V AC. Depends on model/LCD panel size two different types of PSU boards are used:

G1 boards for 26 & 32 inch
G2 boards for 40 & 46 inch

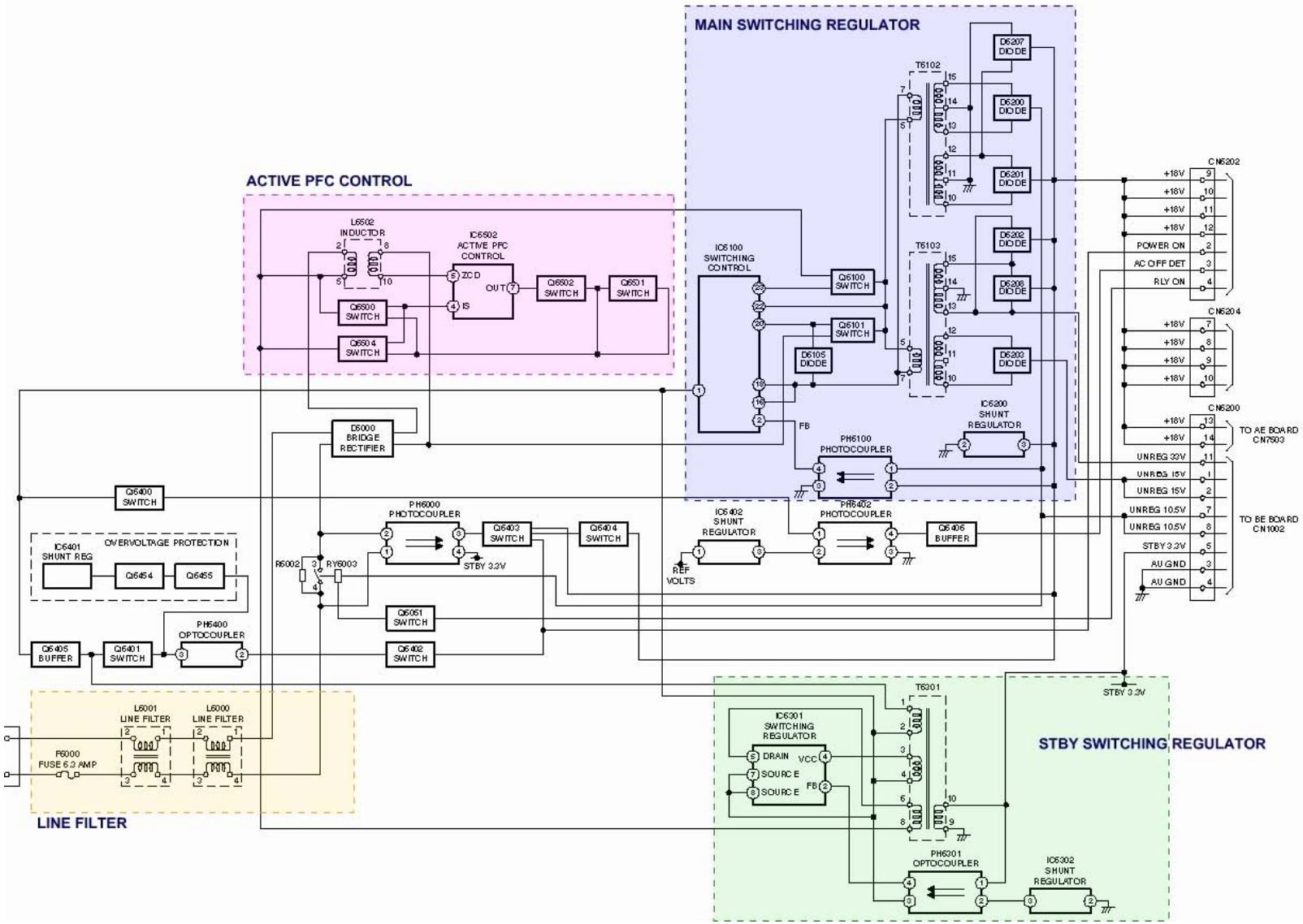
3.2. The main circuits

- **Line Filter**
  This circuit prevents high-frequency signals from going into or coming out of the TV set
- **Active PFC circuit (Power factor correction)**
  The PFC converter is an active filter for improving the power factor by expanding the continuity angle of the power supply input current thus meeting the harmonic current regulation of the power supply.
  This circuit is built around IC6301, L6102, Q6102 (G board) or IC6502, L6502, Q6500, Q6504 (G2 board). The PFC circuit provides a voltage of 390V-400V DC when the TV set works and approximately 310 V DC when the TV set is switched into STBY (measured at cathode of D6506)
- **STBY PSU**
  Simple circuit designed around Switching Regulator MIP2H2 and the transformer T6301.Low number of external parts used. This circuit develops two voltages: 3.3V STBY voltage for devices such as main µPC, EMMA processor, IR receiver and a 17,5V for main converter
- **Main Converter**
  The main converter is a current resonance type converter of half bridge method, and it switches the two MOS-FETs, Q6502 and Q6502, (G1) or Q6100 and Q6502 (G2) alternately ON and OFF by CXD9841M-H (successor of well-known MCZ3001D. This circuit is responsible for the following voltages:
  + 18V Panel voltage
  + 15V AUDIO
  + 33V UNREG
  + 10,5V UNREG
  The main converter circuit is controlled by Microprocessor IC1001 pin32 Power1/Power ON line that is fed to CN6203 pin 2 (G1) or CN6202 pin 2 (G2)
  Depends on the status of the Power ON line the TV set operates or is switched into STBY.
  HIGH – Operation/ **LOW** - STBY

3.3. PSU Block Diagram



3.4. G2 Block Diagram



3.5. STBY Converter

Circuit description
The STBY PSU starts to work as soon as the TV set is plugged - in. It works permanently and can be switched - off only by disconnecting the TV set from the main. It is build around the Switching Regulator IC MIP2H2 and the transformer T6102 (G1) or T6301 (G2).

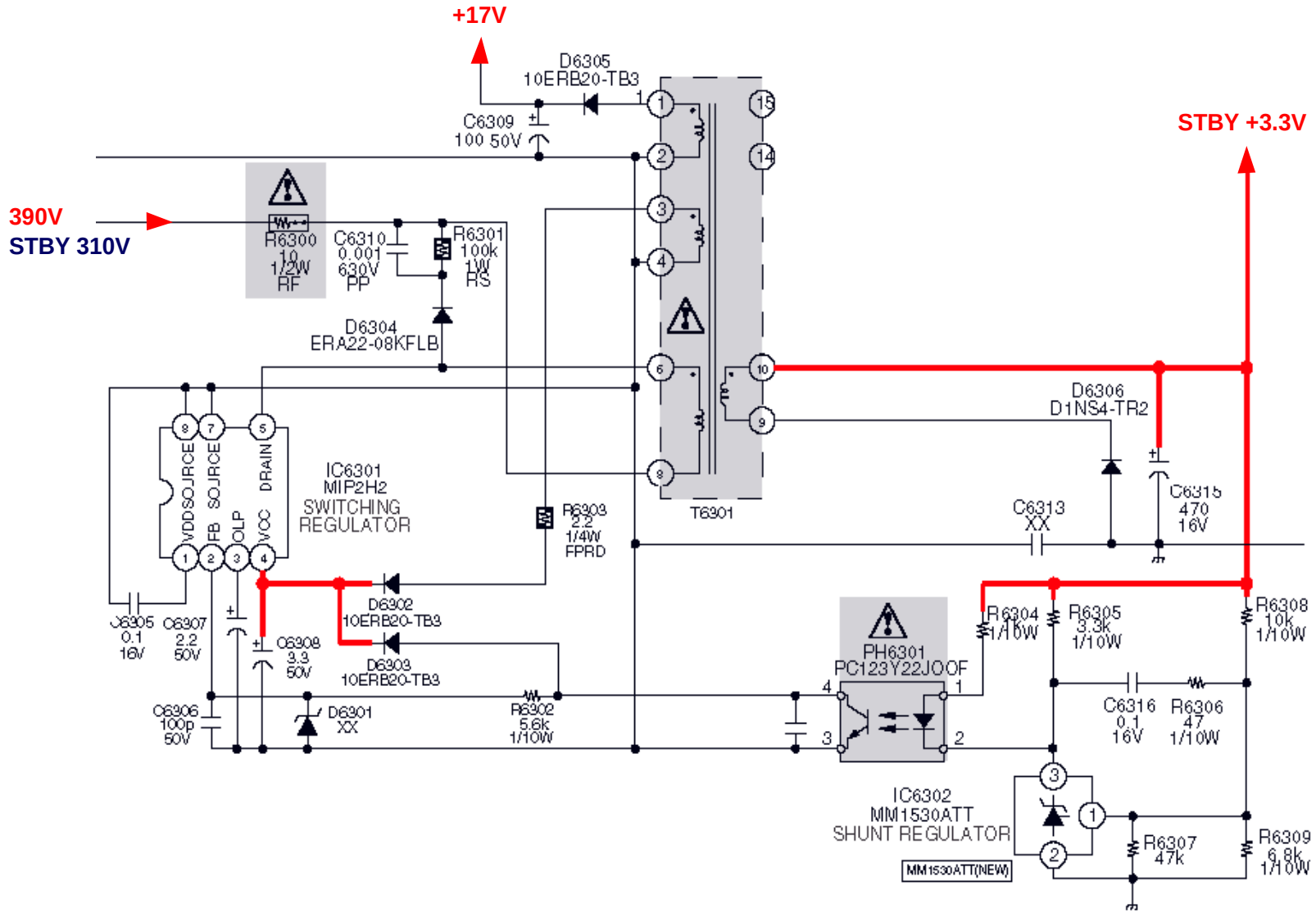
This circuit develops two voltages:
3.3V STBY voltage for devices such as main µPC, EMMA processor, IR receiver and a **17,5V** for main converter (controlled by Power On line).

Control of the output voltages is accomplished by detecting the voltage of
STBY +3.3V output by the shunt regulator IC6201 (G1) or IC6302 (G2) and feeding back to the primary side by the photo coupler PH6102 (G1) or PH6301 (G2).

IC voltage table MIP2H2

PIN	Function	V_{DC}	V_{AC} / Hz
1	VDD	6V	
2	FB	1.8V	
3	OLP	0V	
4	VCC	13V	
5	DRAIN	390V	~500p-p (45kHz)
7-8	SOURCE	GND	

3.5.1. STBY Converter schematic diagram G2 board



3.6. Main Converter

The main converter is a current resonance type converter of half bridge method, and it switches the two MOS-FETs, Q6502 and Q6503, (G1) or Q6100 and Q6502 (G2) alternately ON and OFF by CXD9841M-H (successor of well-known MCZ3001D.
The switching frequency is approx. KHz. The CXD9841M-H has an input voltage detection function, and it detects the voltage resulting from dividing the input voltage at Vsense (pin 1) and operatesLVP and OVP. It also has an OCP function whereby the switching current is detected by R6517 (G1), R6121/6122 (G2) and it controls the output for each pulse of switching when there is over current on the secondary side output due to the over load. Furthermore, when the controlled status stays for a long time, it has a function to completely stop oscillation. Time constant for stopping oscillation is determined by the capacitor connected to the Timer terminal (pin 12). In addition to the above, it also has a feedback open detection function whereby the unregulated condition is detected by the feedback terminal (pin 2) of the IC and the oscillation is stopped at the same time constant as the OCP. When oscillator is stopped at OCP, etc.., it will start again after a certain period of time. However, if such stop and start is repeated 4 times, latching will be caused and stopped condition will be maintained unless the Vcc voltage goes down. D6505 and C6510 (G1) D6103 and C6108 (G2) comprise a boot strap circuit, and it charges C6510/6108 with the voltage Vc2 (pin 17) for gate driving generated inside the IC based on Vcc utilizing the switching if Q6502/6100 to generate gate driving voltage for Q610/Q6502 at the high side. Basically, Vsense terminal is used for ON/OFF. During STBY, oscillation is stopped by compulsorily setting the Vsense terminal LOW by Q6501 (G1) or Q6405 (G2). This ON/OFF function is controlled by Microprocessor IC1001 pin32 Power1/Power ON line that is fed to CN6203 pin 2 (G1) or CN6202 pin 2 (G2). Depends on the status of the Power ON line the TV set operates or is switched into STBY.

HIGH - Operation
LOW - STBY

The signal is transferred to the primary side Q6501 (G1) or Q6405 (G2) by the photo coupler PH6102 (G1) or PH6400 (G2).

IMPORTANT NOTE!

If the STBY mode is executed, the picture and the sound is muted immediately (Panel is switched off also), however the Power On line will stay on the High level for period of time determined by EMMA processor. That means that PSU will definitely be switched to STBY when different voltages are not longer needed e.g. for timer functions or Upgrade Over-The-Air.

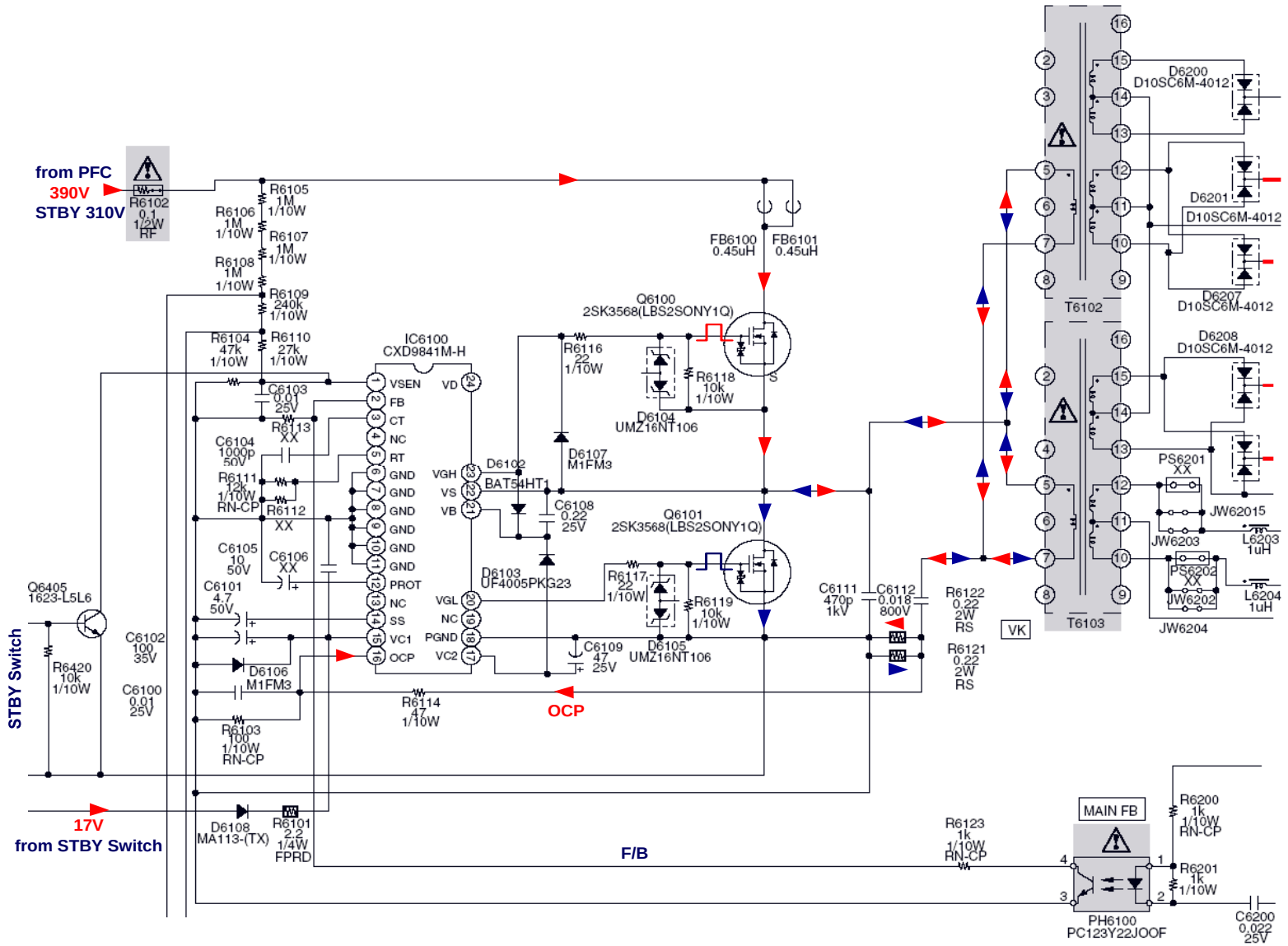
Control of the voltage is accomplished by detecting the voltage of REG18V output by the shunt regulator IC6401 (G1) or IC6200 (G2) and feeding back to the primary side by the photo coupler PH6501 (G1) or PH6100.

Output of the PSU:
UNREG 33V, **UNREG 15V**, **UNREG 10,5V** are the voltages in proportion to the coil turn ratio of the transformer
REG18V output for Inverter board.

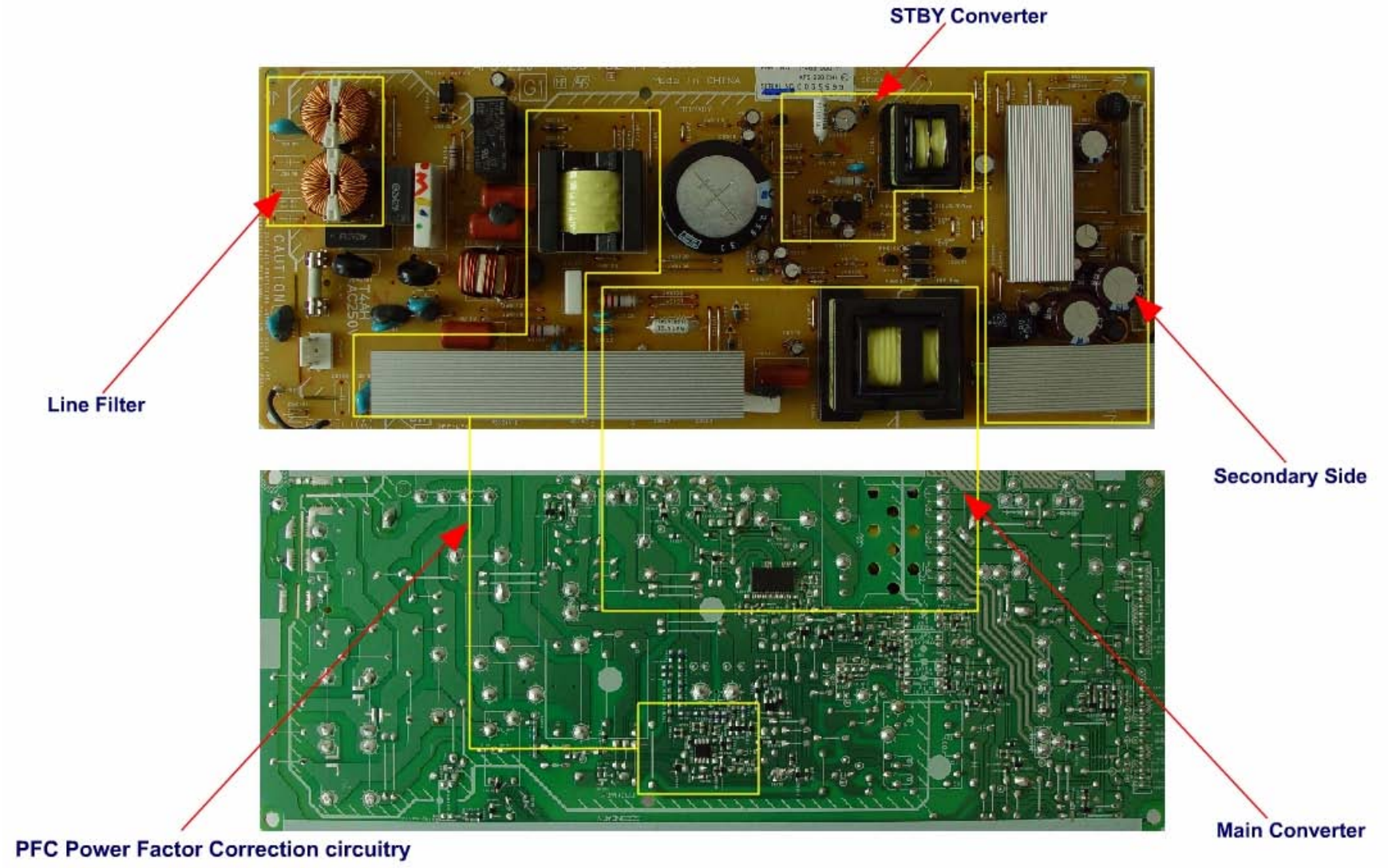
3.6.1. CXD 9841M Pin Function

Pin	Symbol	Description
1	Vsen	Terminal for detection of AC line voltage. For remote ON/OFF, SS Reset and change of OCP
2	FB	Terminal for frequency modulation with FB. Detects FB open
3	Ct	Capacitor determines switching duty and frequency of each protection action
4	NC	NC
5	Rt	Oscillator frequency setting resistor Resistor(Rt) determinates the minimum frequency
6~11	GDN	Ground terminal
12	PROT	Capacitor determinates the period of abnormal detection (OCP,OVP) This determines the intermittent operation time width.
13	NC	NC
14	SS	Capacitor for a soft start timing
15	Vc1	Supply terminal for the control circuit. Start voltage 14,5V, stop voltage 8,5V
16	OCP	Terminal for over current detection and didt protection. Switching frequency becomes high when this terminal detects OCP or didt.
17	Vc2	Output of a supply for a driver 10V
18	PGND	GDN terminal for low side driver
19	NC	NC
20	VG(L)	Output of low side driver
21	VB	Vc2 Supply terminal for high side driver
22	Vs	High side driver reference
23	VG(H)	Output of high side driver
24	VD	Terminal for Drain-Kick starting

3.6.2. Main Converter schematic diagram G2 board



3.6.3. G1 board - circuit's location



4. HYBRID TUNER AND IF STAGE

4.1Circuit description

Universal Front-End (UFE) tuner type BTD-HF431Z is used in WAX 2 chassis.
It is designed for reception of both types of RF signal, Analogue TV RF signal and DVB-T RF signal as well.
The function of the Universal Front-End (UFE) tuner is to select, amplify, and convert the incoming RF signal.

In case of Analogue TV, the RF signal is converted to Video Baseband (CVBS) and Audio Signals such as QSS and FM/AM.
The Video Baseband (CVBS) signal is fed to the AV switch IC CXA 2069Q, and the Audio Signals to MSP4410K.

The Digital Terrestrial (DT) channels are broadcasted using COFDM system.

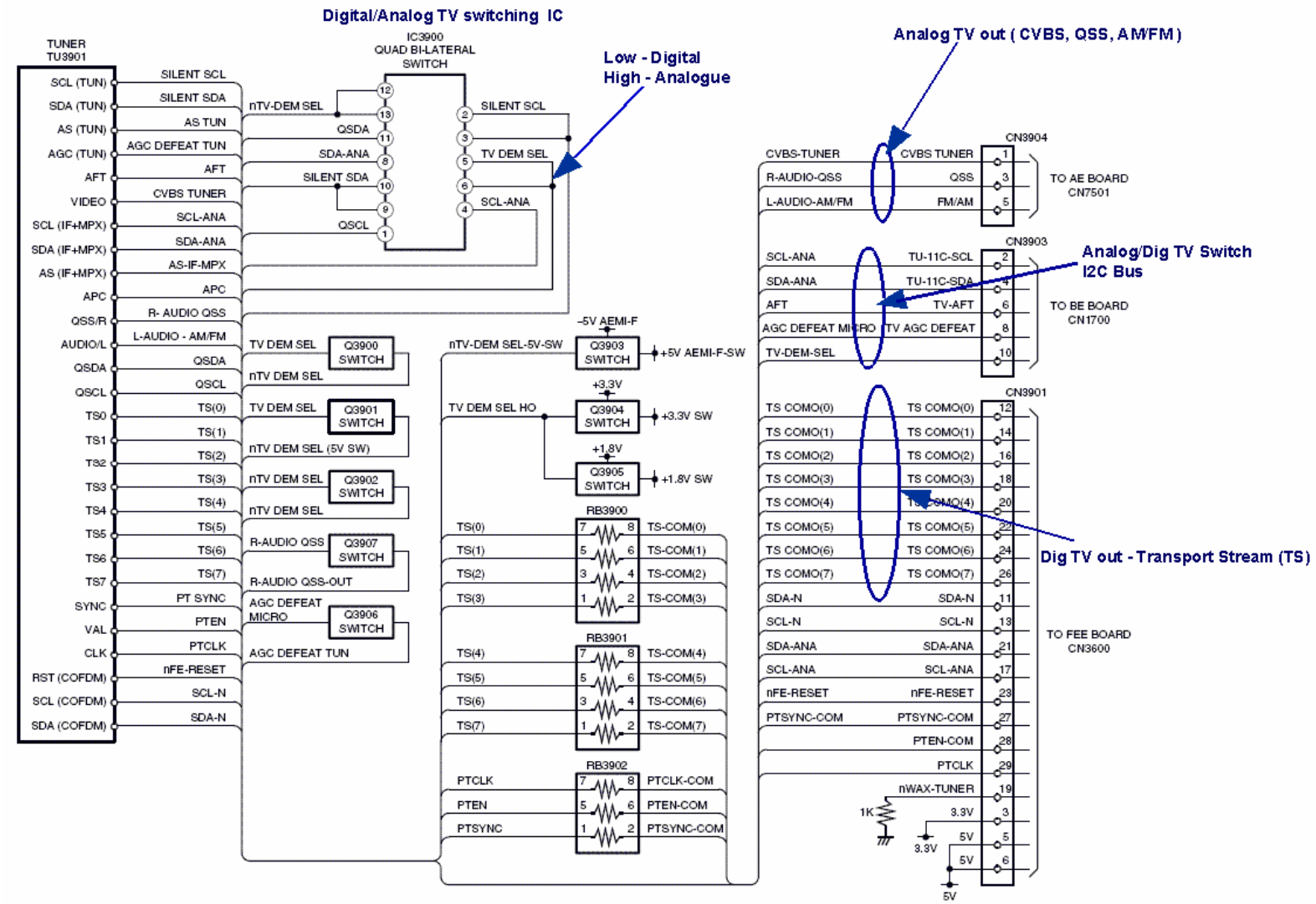
The tuner tunes the required digital channel, and converts the COFDM signal to a base band Transport Stream (TS).

The TS (8 data lines and 4 control lines) contains several digital programs (also called services), usually 4 or 5. This Transport Stream (TS) goes to Multimedia decoder IC3100 EMMA2HL that is placed on the FEE Board.

The Universal Front-End (UFE) tuner can not work simultaneously in digital and analogue mode (DVB-T and Analogue TV).
The operating mode of the hybrid tuner (digital/analogue) can be selected by TV-DEM-SEL line (CN3903 pin 10).
It is controlled by Main Processor IC1001 PIN 80.

Status of pin 80	TV Mode
L	Digital
H	Analogue

4.2. TUE Board - Block diagram



4.3. Hybrid Tuner BTD-HF431Z

(Universal Front-End (UFE) for the whole European market)

Functions

- Hyperband Tuner (45,25MHz ~ 863,25MHz)
- Analogue IF demodulator (systems B/G, D/K, I, L, L')
- COFDM demodulator

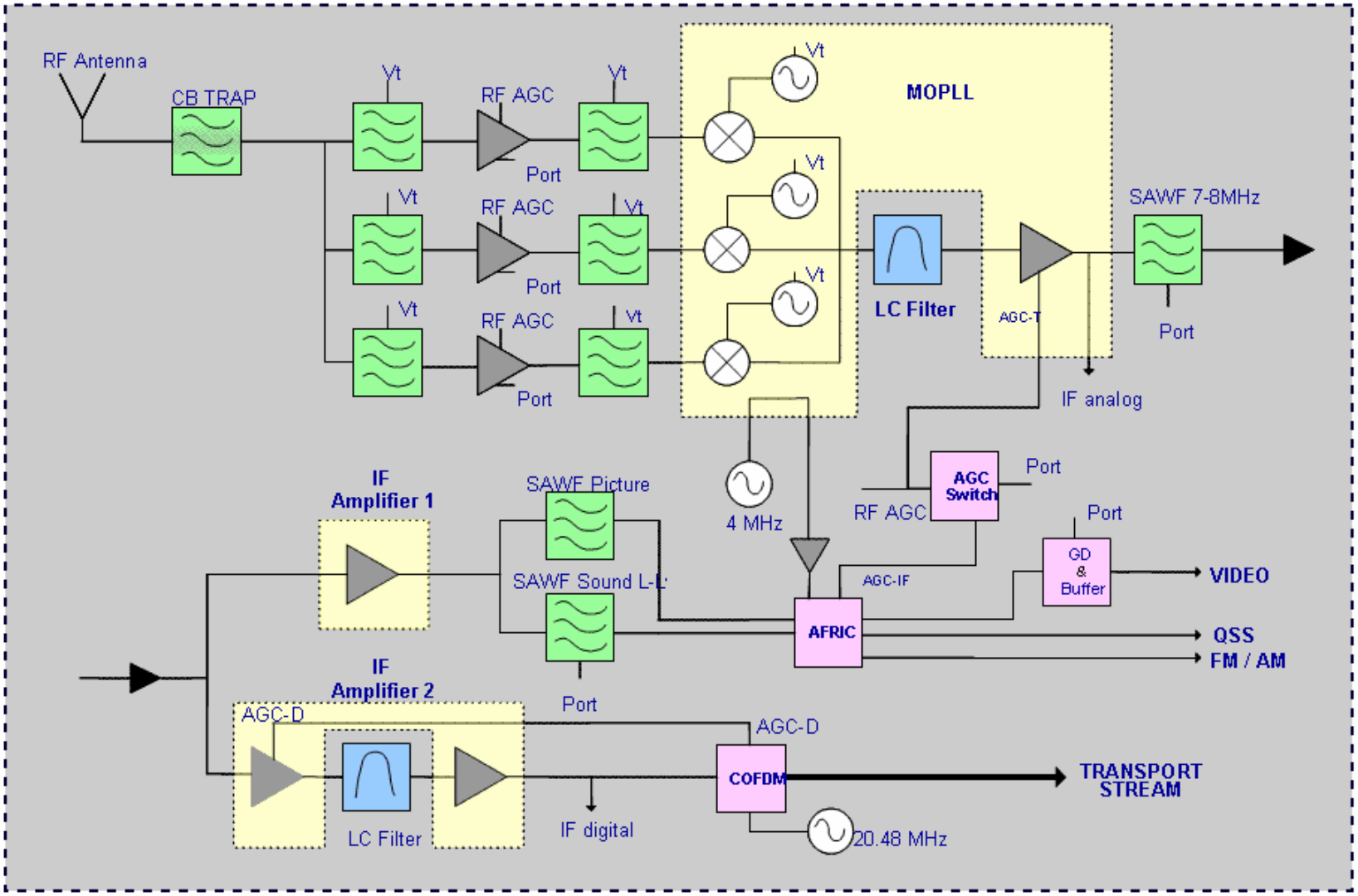
Outputs

- Video Baseband
- QSS
- AM/FM
- Transport Stream
- Suitable for all European countries

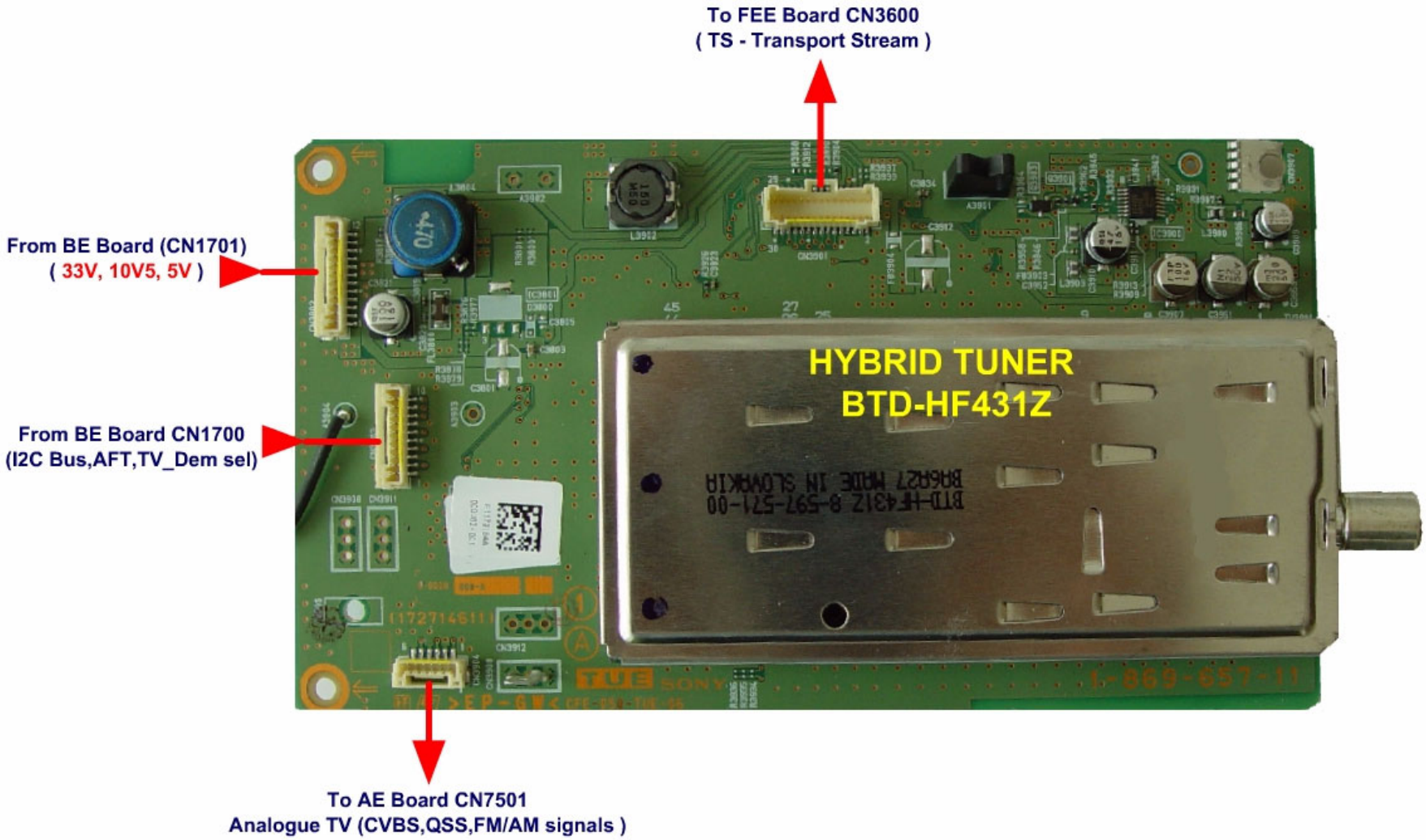
Details

- Switchable SAWF (7/8 MHz) for digital reception
- Switchable audio SAWF for the different TV standards
- Group delay compensation circuit
- MOPLL: TUA6034
- IF amplifier for digital signal: CXA3556
- IF amplifier for analogue signal: TA4019
- Analogue IF demodulator: TDA9886
- COFDM demodulator: CXD1976R
- Three I2C bus connexions (MOPLL/IF demodulator/COFDM demodulator), plus one I2C bus output to be used as quiet I2C from the COFDM demodulator to the MOPLL, through external connexion.

4.3.1. Hybrid Tuner BTD-HF431Z – Block diagram



4.4. TUE Board


To FEE Board CN3600
(TS - Transport Stream)
From BE Board (CN1701)
(33V, 10V5, 5V)
From BE Board CN1700
(I2C Bus,AFT,TV_Dem sel)
HYBRID TUNER
BTD-HF431Z
To AE Board CN7501
Analogue TV (CVBS,QSS,FM/AM signals)

5. MULTIMEDIA PROCESSOR – MPEG DECODER

5.1Circuit description

Transport Stream (TS) from Hybrid Tuner is fed to Multimedia Processor µPD 61123 (EMMA 2L) which is located on the FEE Board. The µPD61123 is a new high performance MPEG decoder for integrated digital television, supporting digital and digitized analogue signals. The µPD61123 integrates two MIPS32™ 4KE™ microprocessor cores capable of delivering speeds of up to 300 MIPS each. The device also offers an improved DDR-SDRAM interface, with speeds of up to 166 MHz and up to 1 GB of memory volume. With the enhanced graphics engine, designers now have even more flexibility to handle advanced graphics and data manipulation. The combination of these performance-enhancing features enables outstanding speed of MHEG interactive applications, smooth operation of MHP, and integration of the standard on-screen display functions.

The µPD 61123 outputs following signals:

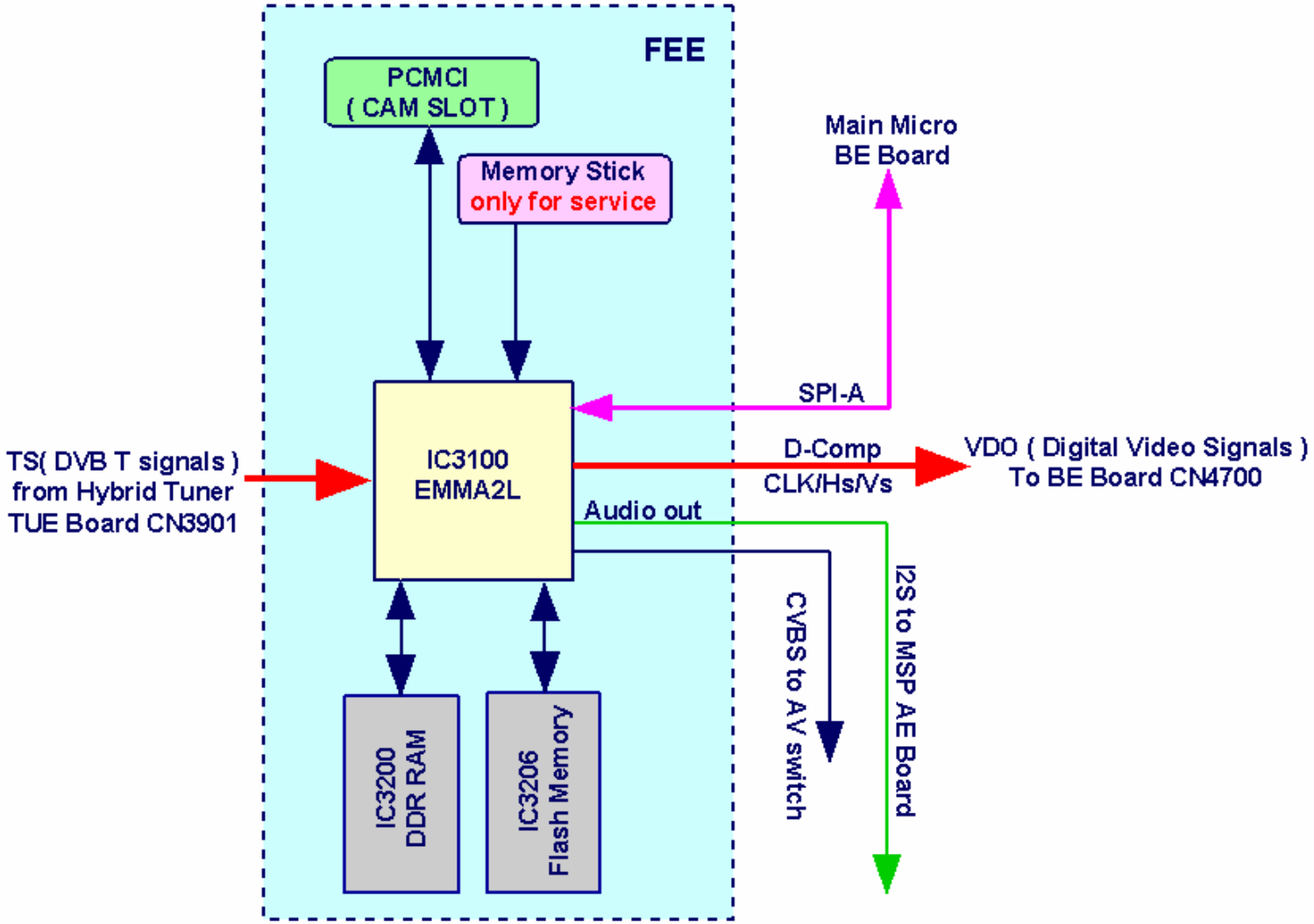
- D-Comp and CLK/Hs/Vs (DVB-T video content) which goes via CN4700 to the Trident IC on the BE Board
- CVBS signal connected to AV switch (this signal is available on SCART 1 and can also be selected on SCART 2)
- Audio I2S signal (**Integrated Interchip Sound** is an electrical serial bus interface standard used for connecting digital audio devices together. It is most commonly used to carry PCM information). The I²S is fed to the Multi Standard Sound Processor MSP 4410K.

The software of the µPD 61123 is written into the Flash Memory (IC3206).
The software upgrade can be done **Over-The-Air** or using Memory Stick
(a special MS slot is located on the FEE Board)

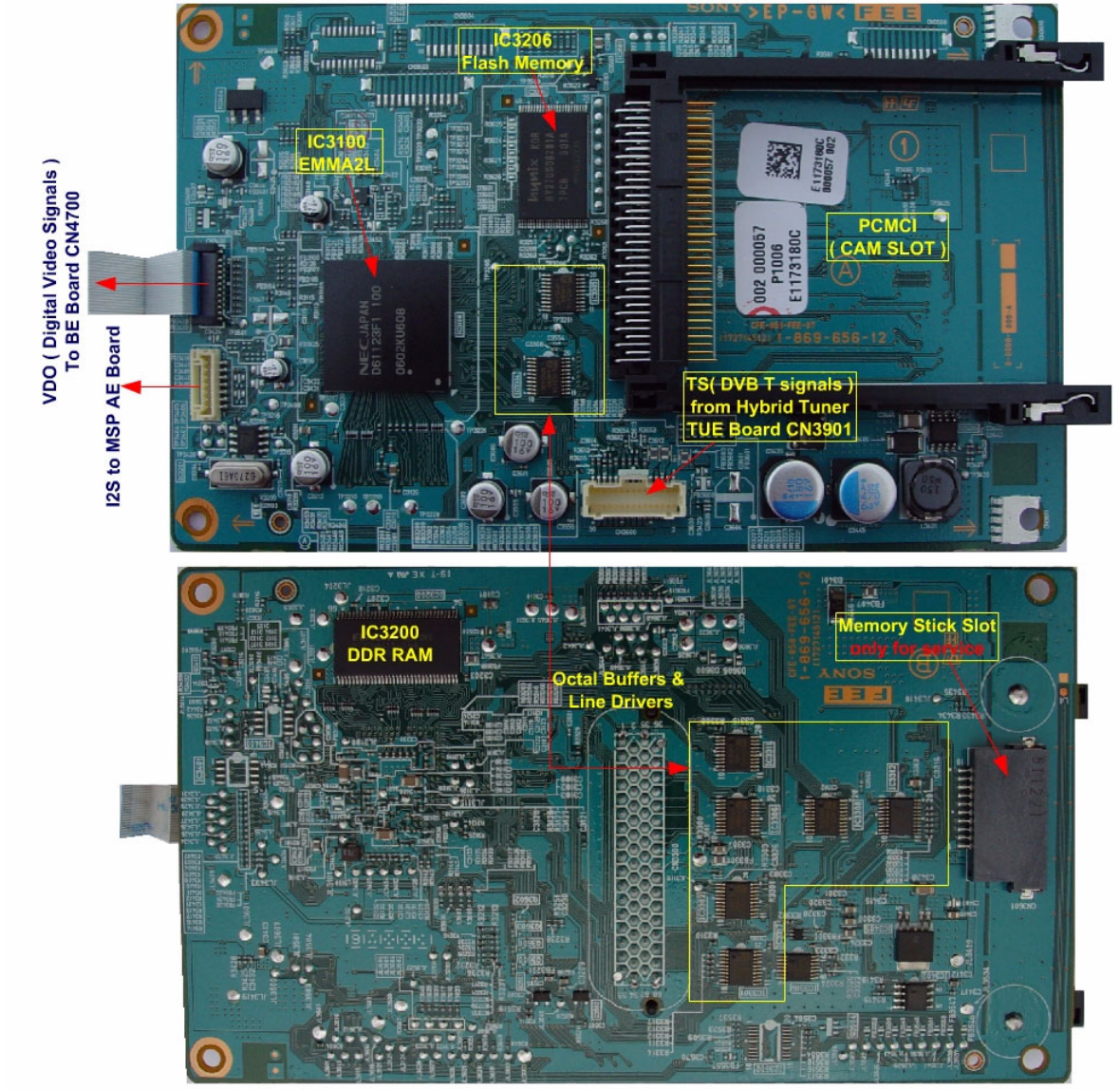
Other devices on the FEE board:

- IC3200 EDD1216AATA-6B-E DDR SDRAM - used by EMMA 2L
- IC3301-3312 74LVC541APW BUFFER & LINE DRIVER – interface between PCMCI and Multimedia Processor
- CAM Slot – for PCMCI

5.2. Circuit – Block diagram



5.3. FEE Board


IC3206
Flash Memory
IC3100
EMMA2L
PCMCI
(CAM SLOT)
VDO (Digital Video Signals)
To BE Board CN4700
I2S to MSP AE Board
TS(DVB T signals)
from Hybrid Tuner
TUE Board CN3901
IC3200
DDR RAM
Octal Buffers &
Line Drivers
Memory Stick Slot
only for service

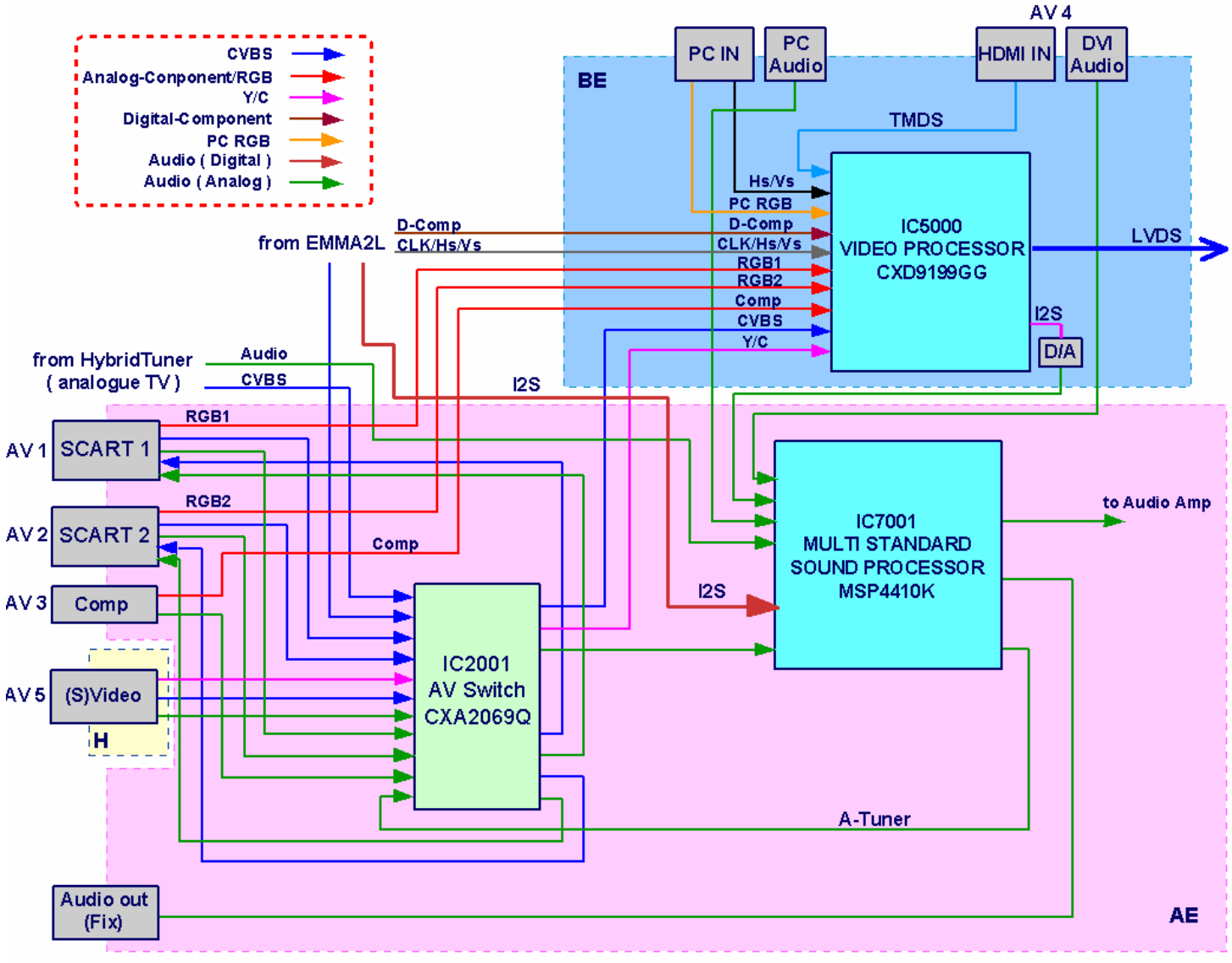
6. AUDIO/VIDEO SWITCHING

6.1. Circuit description

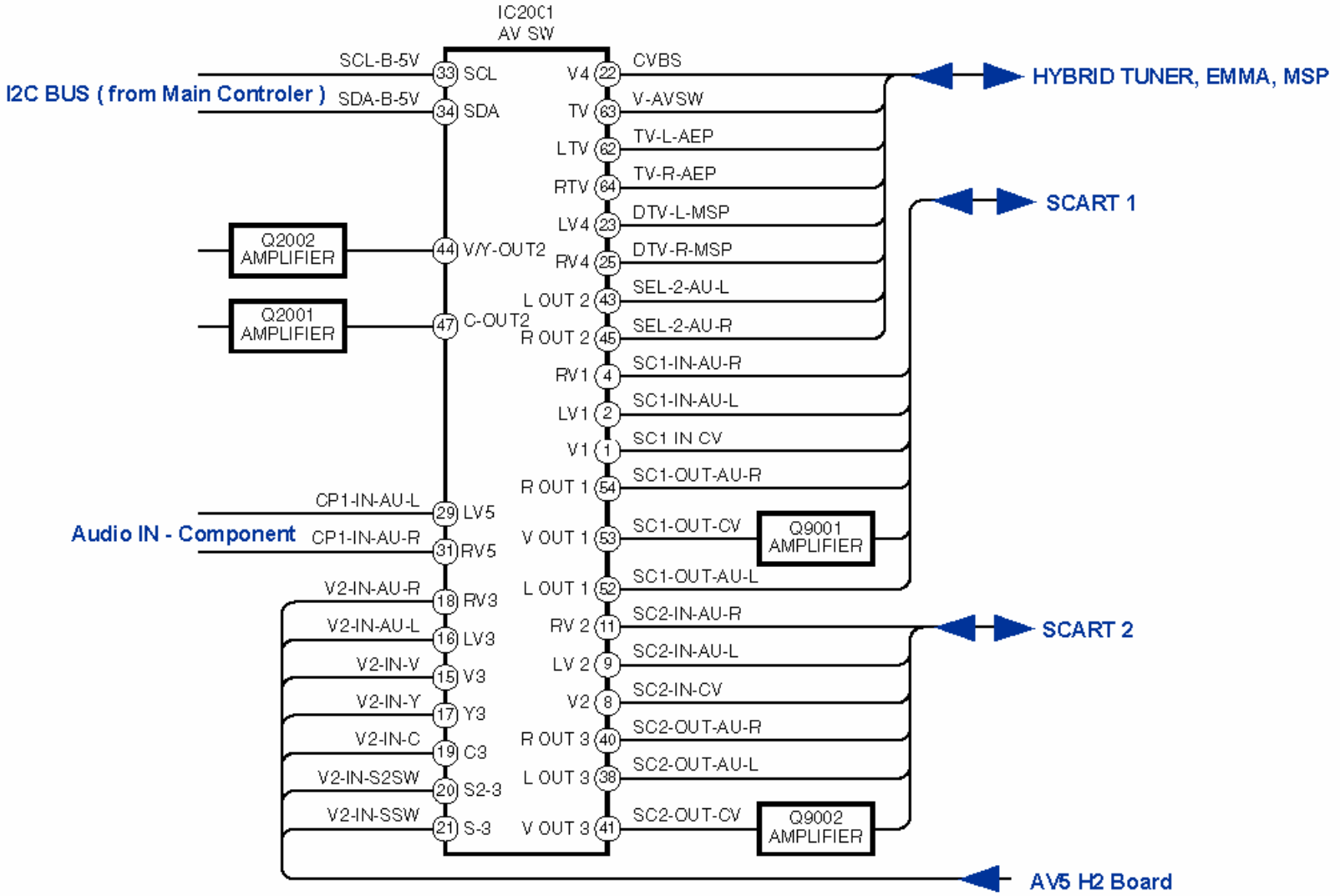
Apart from DVB-T and Analogue TV HF signals, modern TV set must be able to receive video and audio signals from different external sources, such as DVD players, STBs, camcorders, PCs,
Therefore several different types of terminals/ interfaces are needed.
The WAX2 chassis meets the requirements and offers the following selectable Input/Output terminals:
AV1 - Inputs for Audio and Video (CVBS) signals, Inputs for RGB.
Outputs of TV Video and Audio signals (from Hybrid tuner)
AV2 - Inputs for Audio and Video (CVBS) signals, Inputs for RGB.
Selectable outputs of TV Video and Audio signals (TV from tuner, AV1, AV5, Auto)
Smartlink Interface.
AV3 - Component input signal through the Y, PB/CB, PR/CR sockets and audio input signal through the L, R sockets
AV4 - Digital audio/video signal is input through the HDMI IN 4 socket.
Audio input signal is analogue only if the equipment has been connected using the DVI and audio IN socket.
AV5 - Video input (CVBS) signal through the video socket, and audio input signal through the L (MONO), R audio sockets
S video (appears only if the equipment is connected to the S video socket)
PC IN - 15 Pin D-Sub Connector.
CAM - Conditional Access Module
Due to the high number of Audio and Video signals which have to be controlled, three ICs have been involved in this switching process, IC 2001(AV Switch CXA 2069Q), IC 7001(MSP 4410K) both on the AE board and IC 5000 (Video processor) on the BE board.
Switching of Video signals:
All CVBS input signals and the Y/C input are connected to AV Switch CXA2069Q.
Selected in this IC signal is fed to Video processor IC 5000. AV Switch IC is also responsible for output of the CVBS signals for AV1 and AV2.
All other signals such as RGB1, RGB1, Component signal, D- Comp from EMMA, TMDS from HDMI interface and the PC IN signal are connected directly to the Video processor.

Switching of Audio signals:
Audio signal from AV1, AV2, AV3 and AV5 go to the AV Switch IC 2001, selected signal is fed to MSP
All other Audio signals (from Hybrid tuner, PC IN, DVI IN, HDMI IN) are connected directly to MSP

6.2. AV Switching – Signals flow



6.3. AV Switch CXA 2069Q – Block Diagram



6.4. CXA 2069Q – Pin configuration & Features

Description

The CXA2069Q is a 7-input, 3-output audio/video switch featuring I2C bus compatibility for TVs. This IC has input pins that are compatible with S2 protocol.

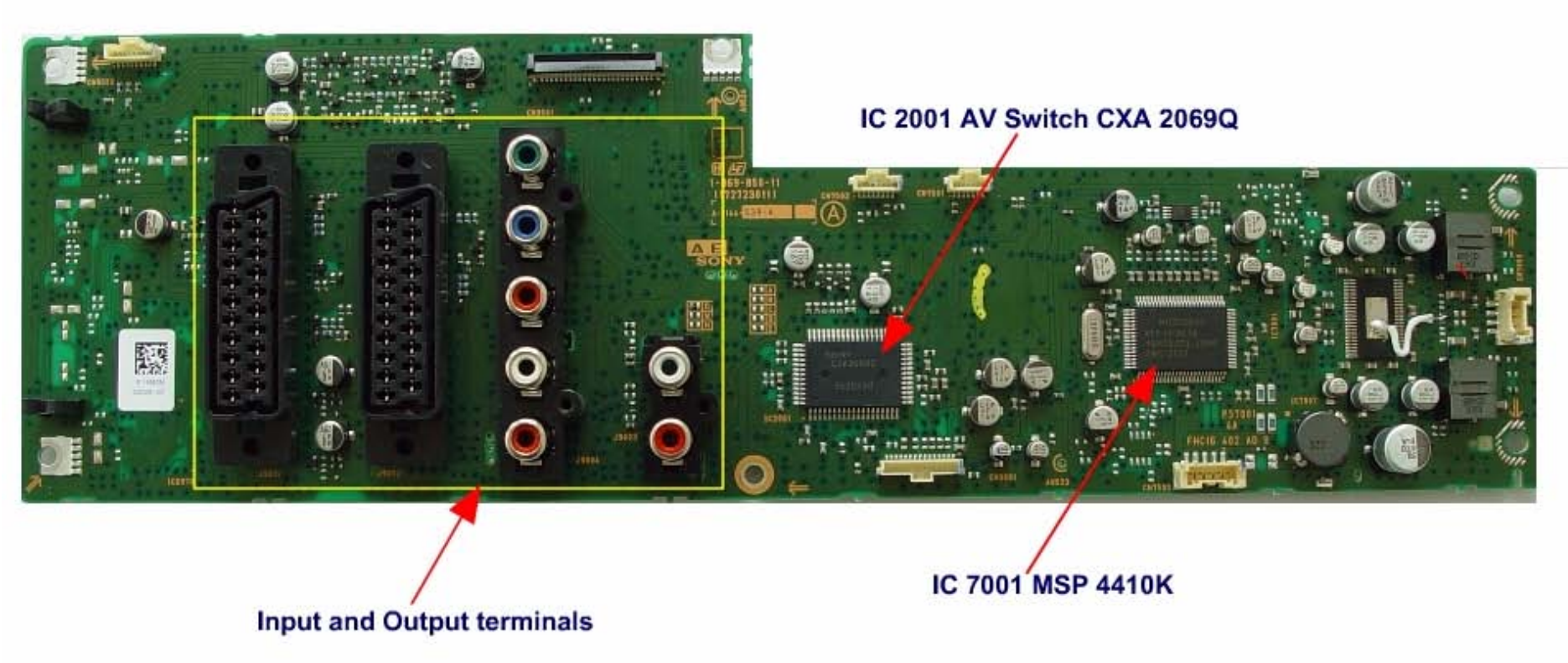
Features

- 4 inputs that are compatible with S2 protocol
- Serial control with I2C bus
- 7 inputs, 3 outputs
- The desired inputs can be selected independently for each of the 3 outputs
- Wide band video amplifier (20 MHz, –3 dB)
- Y/C MIX circuit
- Slave address can be changed (90H/92H)
- Audio muting from external pin
- High impedance maintained by I2C bus lines (SDA, SCL) even when power is OFF
- Wide audio dynamic range (3 Vrms typ.)

Applications

Audio/video switch featuring I2C bus compatibility for TVs

6.5. AE Board


IC 2001 AV Switch CXA 2069Q
IC 7001 MSP 4410K
Input and Output terminals

7. VIDEO PROCESSING

7.1. Circuit description

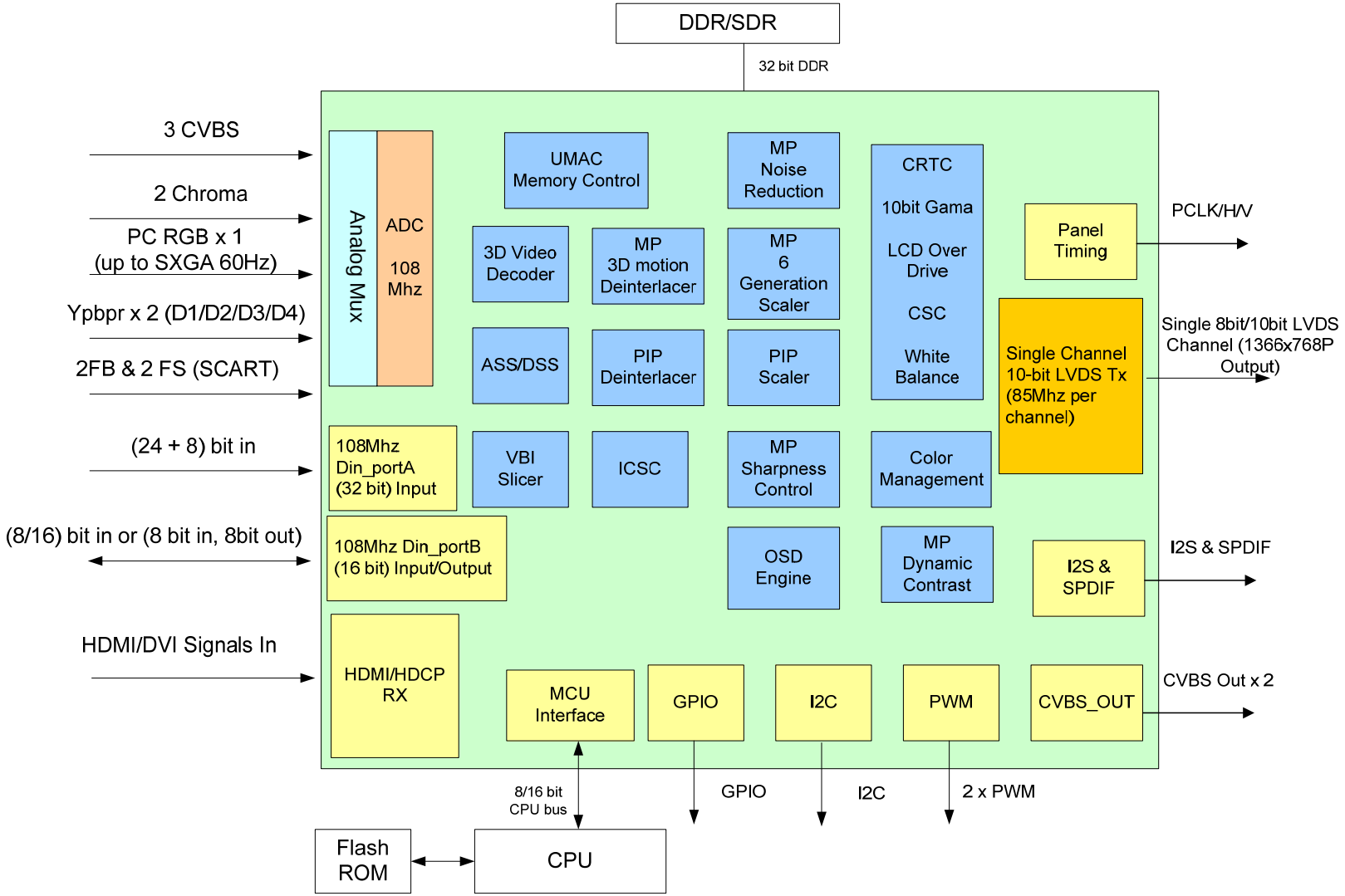
The complete Video Process is performed within the Video Processor CXD9199GG (Trident SVP™PX) on the BE Board.
Different video signals such as CVBS, Y/C, RGB, Component, PC RGB, HDMI/DVI or D-comp from Emma processor are fed to the CXD 9199GG in order to be process.
The CXD9199GG video processor is a highly integrated system-on-a-chip device, targeting the converging HDTVready and PC-ready LCD TV, PDP TV, and DLP TV applications where high precision processing of video and data are the requirements. SVP™PX contains 6th generation dual-purposed triple 10-bit high-precision and high speed video ADCs for both PC and video inputs, the high speed HDMI could support all HDMI inputs up to 135 MHz with HDCP format, the high-performance multi-format 3D digital comb video decoder that supports NTSC,PAL, and SECAM (only 2D) , a HDTV sync separator, motion adaptive de-interlacing engine, and the video format conversion engine, supporting multi-window display in many different output modes.
Trident's DCRe™ – Digital Cinema Reality engine, is integrated inside the SVPPX family to provide the most natural cinema-realistic images. The DCRe™ technology integrates advanced 3D-comb video decoding, advanced motion adaptive de-interlacing, object-based digital noise reduction, advanced 6th generation scaler, film mode support, average picture level (APL), edge smoothing and dynamic sharpness enhancement. Trident's patented Unified Memory Architecture (UMA) that allows frame rate conversion, 3D comb video decoding, and video enhancement processing to share the same memory buffer that is made up of high-speed and cost-effective PC graphic memory. All these advanced digital processing techniques combined with a true 10-bit video data processing for the most optimal video fidelity to provide the most natural and cinema quality video images.
Designed for maximum system design flexibility, SVP™PX integrates all video interfaces to support converging digital video, analogue video, and PC data applications. The users of Trident's single chip SVP™PX series video processor(s) will benefit from many features while maintaining a price competitive advantage over the existing solution

SVP PX FEATURES

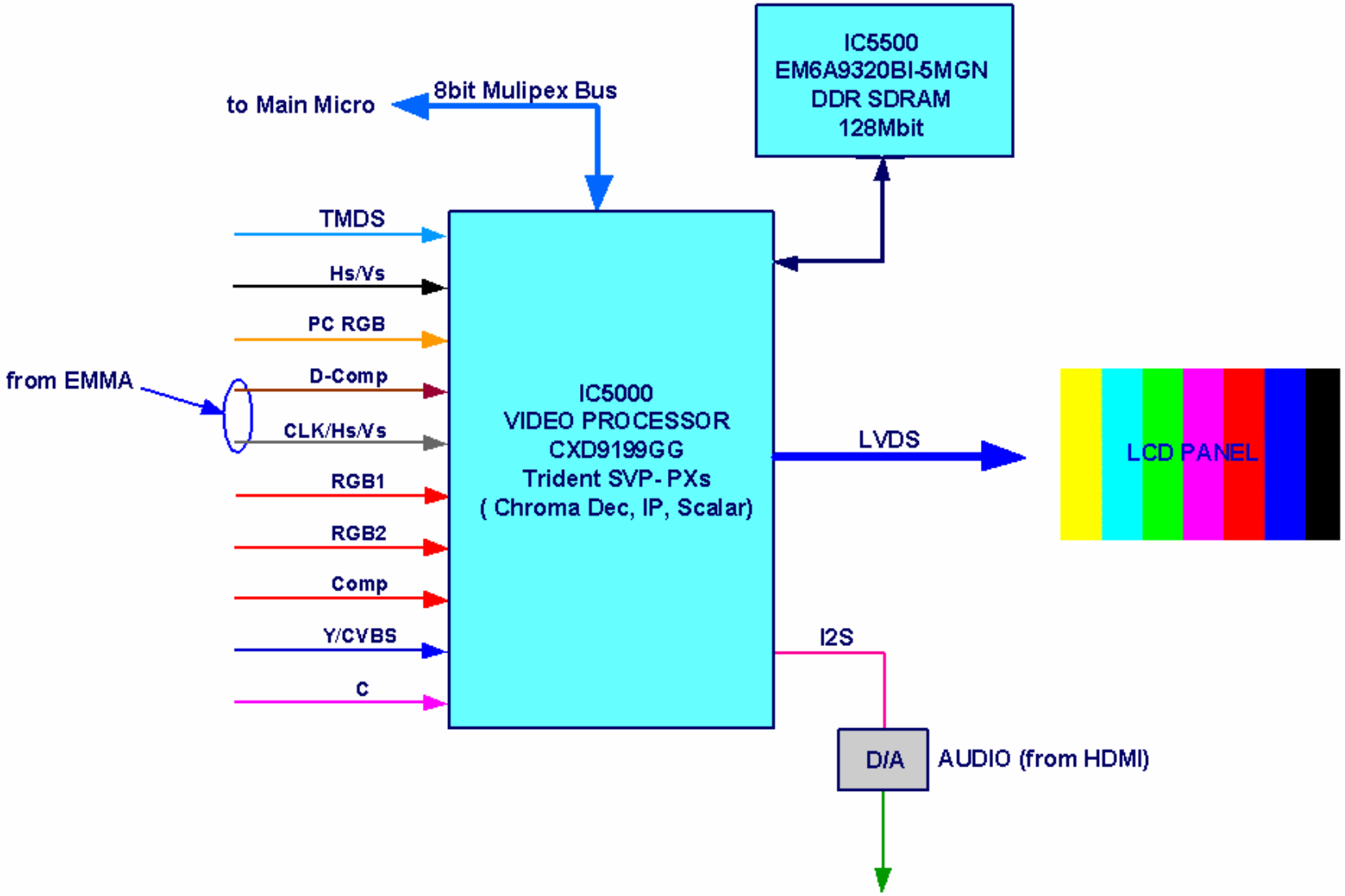
- Integrated HDMI/DVI Receiver with HDCP up to 135 MHz
- High-quality Single-channel HD/SD de-interlacing/scaler
- Real 10-bit whole chip processing
- High bandwidth processing to support 1080i and SXGA video input and output up to 1366x768.
- Blue-stretch; Green-stretch; Skin-color correction with three fully programmable color region processing.
- Enhanced Dynamic Contrast
- Two Turbo OSD w/ 2D-Gfx acceleration
- 10-bit 108Mhz ADC & 10-bit 2D/3D color decoder

- Advanced content-adaptive noise reduction
- MPEG Noise Reduction for MPEG video signal input
- Vertical keystone & H/V-Mirror & H/V-Panorama in dual channels
- Fully programmable sRGB & white-balance
- Teletext
    - TCD3 decoder has built-in teletext data slicer that decodes and has an OSD page display up to 4.5K page 75Hz
    - Supports Teletext 2.5 Spec.
- Both PC and HD motion picture support auto-phase adjustment/auto-mode detection
- Built-in Single 8bit / 10 bit LVDS transmitter
- Enhanced H & V sharpness and LCD over drive
- Integrated ADC
    - High-precision 10-bit ADC mode up to 108 MHz for SD/HD analogue video input modes
    - Direct support for CVBS/S-Video/Component and HD-D1/D2/D3/D4 modes
    - Decode FB and FS signals for fully SCART factions
- Integrated 6th Generation Motion Adaptive 3D Digital Comb Video Decoder with Programmable Filter
    - Supports NTSC, PAL, and SECAM formats
    - Smooth 3D/2D image transition with Trident's proprietary object and motion adaptive detection
    - Programmable comb filter adapts to all possible environments, and 2D Y/C separation
    - Colour edge enhancement circuit improves the chroma transient so that the chroma edge looks sharper than the original signal
    - High precision 10-bit ADC analog front-end
    - Enhanced NTSC/PAL/SECAM auto detection
    - Enhanced false colour reduction circuitry
- Memory Interface
    - Supports 16/32 bits DDR or SDR memory interface
    - Memory clock support up to 166 MHz
    - Wide memory size supported up to 16 MB

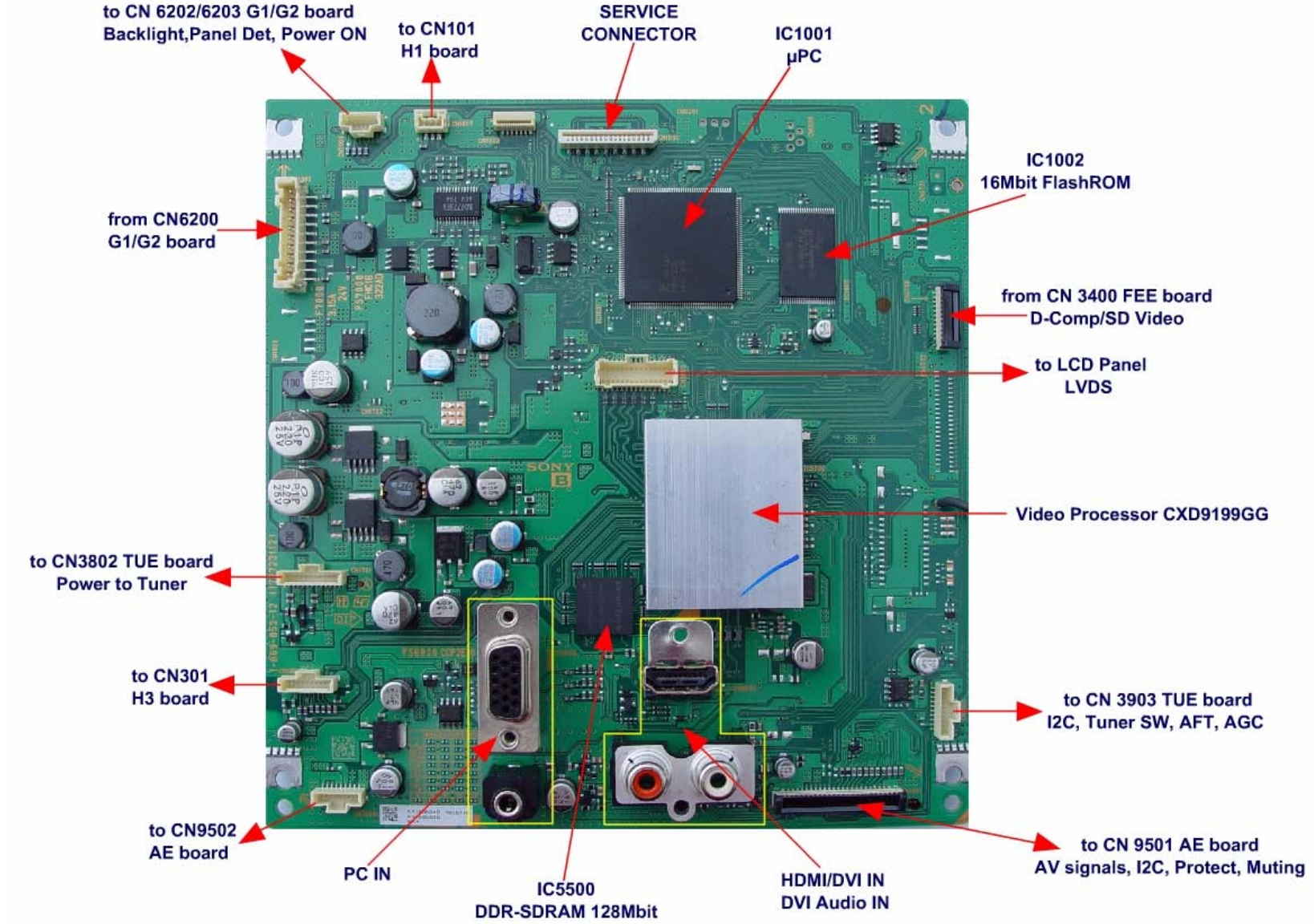
7.2. SVP PX Block Diagram



7.3. Video Processing – Block diagram



7.4. BE Board


to CN 6202/6203 G1/G2 board
Backlight,Panel Det, Power ON
to CN101
H1 board
SERVICE
CONNECTOR
IC1001
µPC
IC1002
16Mbit FlashROM
from CN6200
G1/G2 board
from CN 3400 FEE board
D-Comp/SD Video
to LCD Panel
LVDS
Video Processor CXD9199GG
to CN3802 TUE board
Power to Tuner
to CN301
H3 board
to CN 3903 TUE board
I2C, Tuner SW, AFT, AGC
to CN9502
AE board
PC IN
IC5500
DDR-SDRAM 128Mbit
HDMI/DVI IN
DVI Audio IN
to CN 9501 AE board
AV signals, I2C, Protect, Muting

8. AUDIO PROCESSING

8.1. General Circuit Description

Modern TV set must also be able to process many audio signals come from different sources. It should support both, analogue and digital audio signals. WAX2 chassis meets all the requirements using a well-known Multi Standard Sound Processor MSP4410K.
All types of audio signals coming from different inputs such as HDMI, DVI, PC, Hybrid tuner, EMMA processor or AV switch are fed to the Multi Standard Sound Processor. The MSP processes all the signals and controls the volume, balance, bass, treble, loudness of the Loudspeaker / Headphone channels.

The Sound Processor outputs the following audio lines:

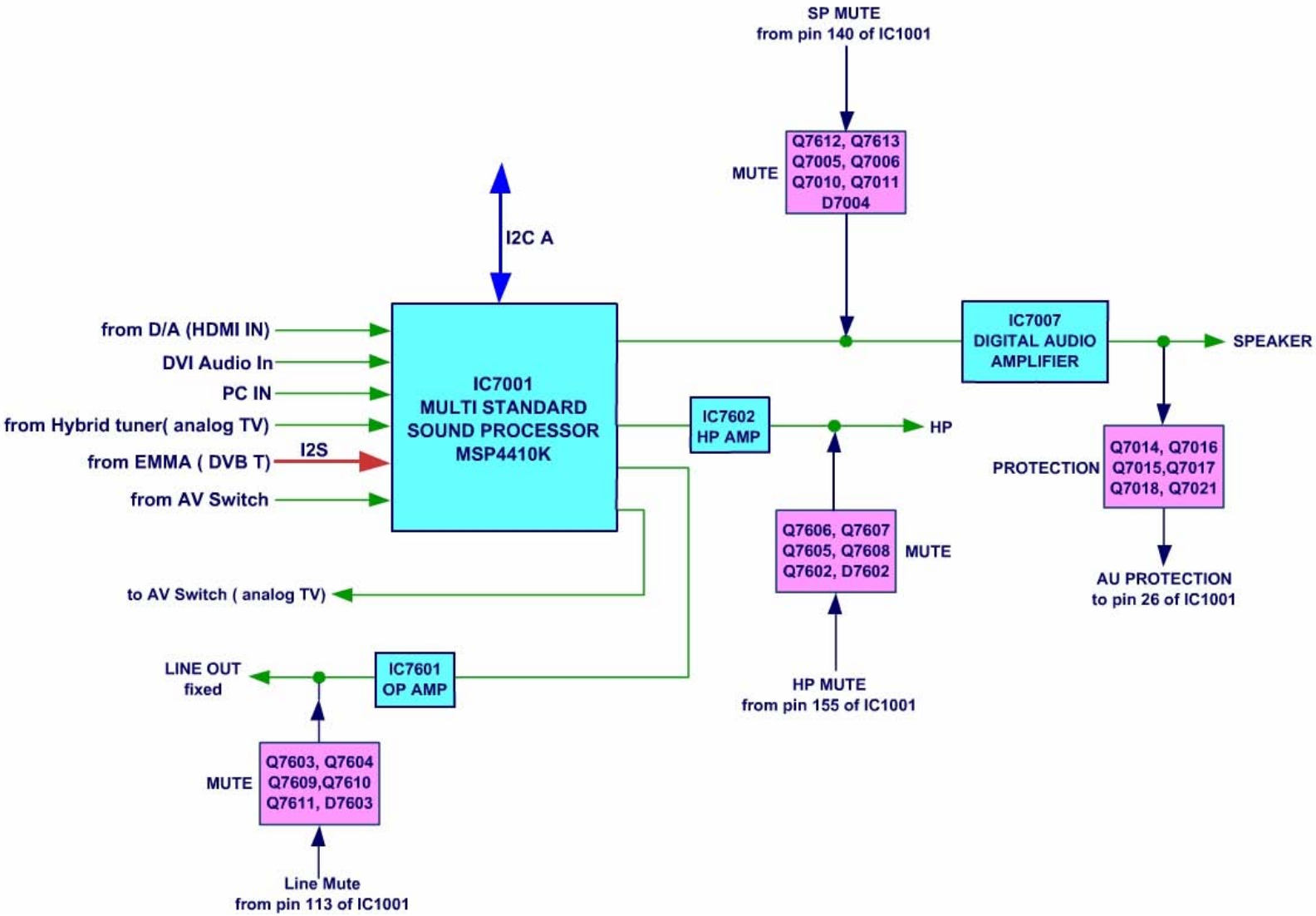
Main Speakers Audio Output (pins 27, 28) which is fed to the IC7007 M6157 Digital Audio Amplifier.
A Speaker Muting Circuit (SP_MUTE) is connected the Main Speakers Output lines.
This muting circuit is controlled by pin 140 of Micro Processor.
The Output of the Digital Audio Amplifier is protected by Speaker Protection Circuit (AU-PROT.)
It prevents the Speakers from damage. This circuit monitors the output of the Amplifier.
As soon as DC voltage is detected the Micro Processor is informed via AU-Prot line (pin 26) and the TV set will be switched off.

Headphones (HP) Output (pins 24, 25) with independent volume controls.
The HP output signals are amplified by small buffer IC7602 and finally supplied to the Headphones jack on the H2 board.
This HP line is controlled by a muting circuit" HP MUTE" which is connected to the pin 155 of the Micro Processor

LINE OUT (pins 36, 37) is a fixed audio signal amplified by IC7601 and supplied to the Audio Output.
This Audio Output is controlled by a separated muting circuit as well. It is a LINE MUTE circuit fed to pin 113 of Micro Processor

Analog Tuner Audio Output .One more audio output is provided by MSP. It is audio signal from analogue tuner (which has to be fed back to the AV Switch IC in order to be available on the Scart connector.

8.2. Audio Processing – Block Diagram



8.3. MSP4410K

8.3.1. General Description

The Multistandard Sound Processor MSP4410KSound Processors covers the sound processing of all analog TV-Standards worldwide, as well as the NICAM digital sound standards and FM stereo radio. The full TV sound processing, starting with analog sound IF signal-in, down to processed analog AF-out (baseband audio), is performed on a single chip. With its extended number of inputs and outputs, the MSP 4410K can handle all audio signals in modern LCD, PDP, or CRT TVs. Even additional signals from Digital TV decoders are included in the MSP 4410K chip TV Audio concept. The MSP 44/46xyK has an internal 40 ms (stereo) audio delay line. Complex video processing delays the picture by several video frames. To avoid mismatch between sound and a speaker's lip movement, the audio has to be delayed accordingly (lip sync). If longer delays are required, an additional external delay IC has to be used.

The MSP 4410K built-in stereo A/D converters offer a S/N ratio of 95 dBA typ. The multiple D/A converters with analog volume and 0.125 dB steps make use of the Micronas unique multibit Delta-Sigma technology, offering a dynamic range of 95 dBA typically.

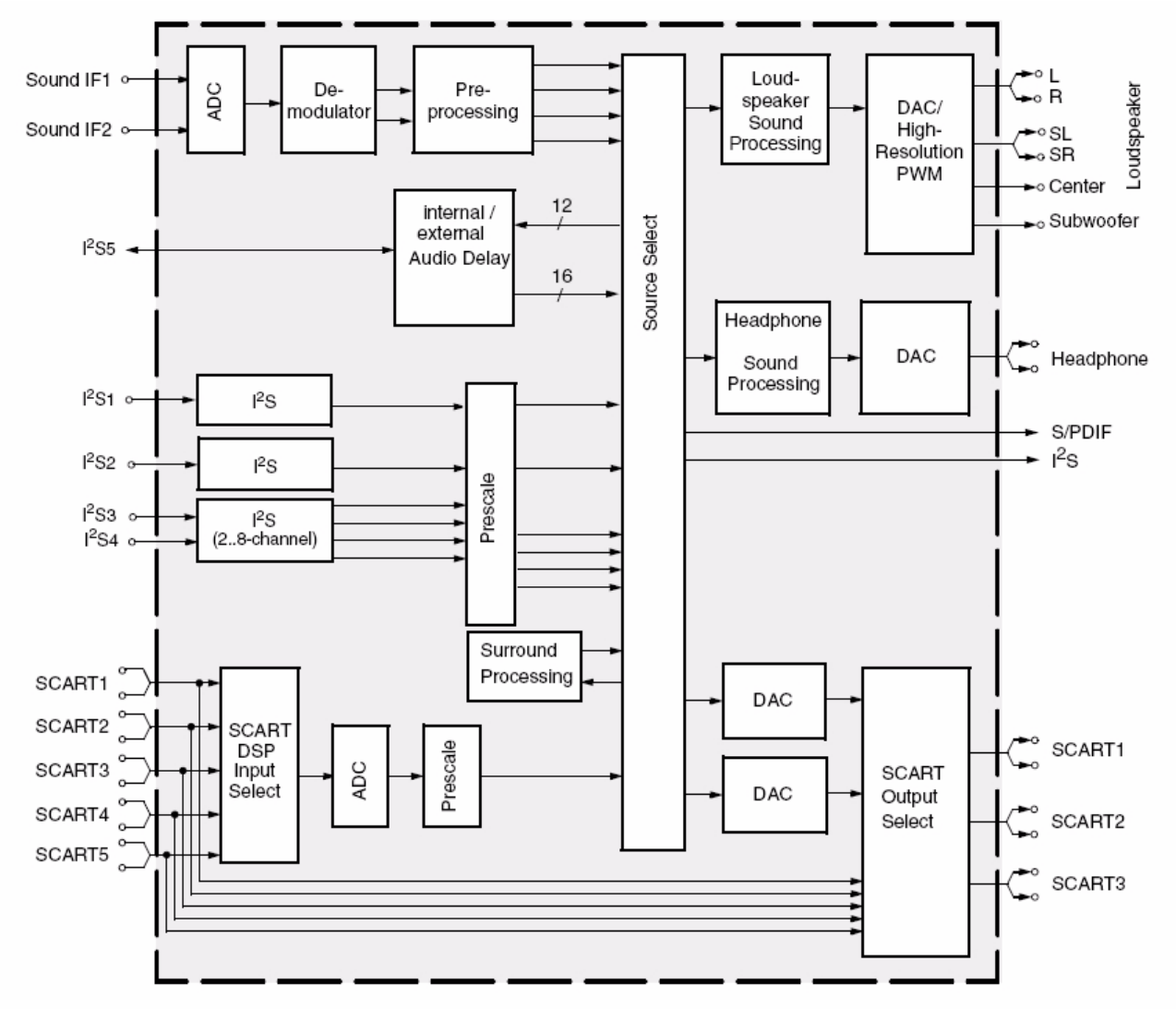
The DSP processing is performed at 48 kHz sample rate, maintaining the full audio bandwidth of 20 kHz.

These TV sound processing ICs include versions for processing the multichannel television sound (MTS) signal conforming to the U.S. standard recommended by the Broadcast Television Systems Committee (BTSC). The DBX noise reduction, or alternatively, Micronas Noise Reduction (MNR) is performed alignment free. Apart from all 2-carrier standards, other processed standards are the Japanese FM-FM multiplex standard (EIA-J) and the FM Stereo Radio standard. The MSP 4410K provides optimum stereo performance without any adjustments. The MSP 4410K offers the following automatic functions:

– ASD (Automatic Standard Detection) detects the actual broadcasted TV standard automatically.
– ASS (Automatic Sound Select) switches automatically (without any I2C action) between mono/stereo/ bilingual when the broadcast mode changes.

The MSP 44/46xyK can handle very high FM deviations. The MSP 4410K has all functions of the MSP 44x0G with additional multichannel outputs, S/PDIF output, Dolby ProLogic II, internal Audio Delay Line and interface to an external Audio Delay. In general, outline dimensions, electrical characteristics, and application diagrams are identical to the MSP 44x0G.

8.3.2. Simplified functional block diagram of the MSP 4410K



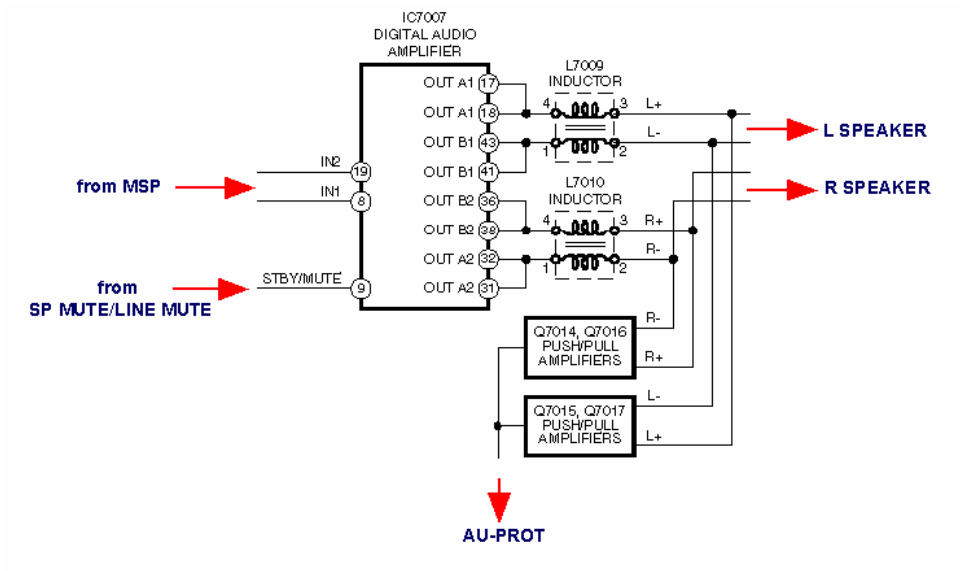
8.3.3. MSP4410K Main Features

- Differential PWM Driver Outputs for Loudspeaker channels
- internal Lip Sync Delay Line
- 8-channel I2S Interface to external audio delay line
- S/PDIF output (PCM stereo, 48 kHz)
- 48 kHz sampling rate (audio bandwidth 20 Hz ... 20 kHz)
- Upsampling of I2S input to 48 kHz
- Standard Selection with single I2C transmission
- Interrupt output programmable (indicating status change)
- Loudspeaker / Headphone channel with volume, balance, bass, treble, loudness
- AVC: Automatic Volume Correction
- Subwoofer output with programmable low-pass and complementary high-pass filter
- Micronas BASS (MB) and 7-band graphic equalizer for loudspeaker channels
- 3-Band Parametric Equalizer for left/right loudspeaker channels
- Five Stereo SCART (line) inputs; three Stereo SCART outputs 1)
- Complete SCART in/out switching matrix
- Four Stereo I2S inputs; one I2S output
- One 8-channel asynchronous I2S input
- I2S output with 8-channel capability
- BBE Multi-Channel High Definition Sound (optional)
- SRS TruSurround XT (optional)
- BBE VIVA (optional)
- ASD: Automatic Standard Detection of analog TV standards/Automatic Carrier Mute function
- ASS: Automatic Sound Selection (mono/stereo/bilingual)
- Two selectable sound IF (SIF) inputs
- Automatic Carrier Mute function
- All analog Mono sound carriers including AM-SECAM L
- All analog FM-Stereo A2 and satellite standards
- Adaptive deemphasis for satellite (Wegener-Panda, acc. to ASTRA specification)
- All NICAM Standards

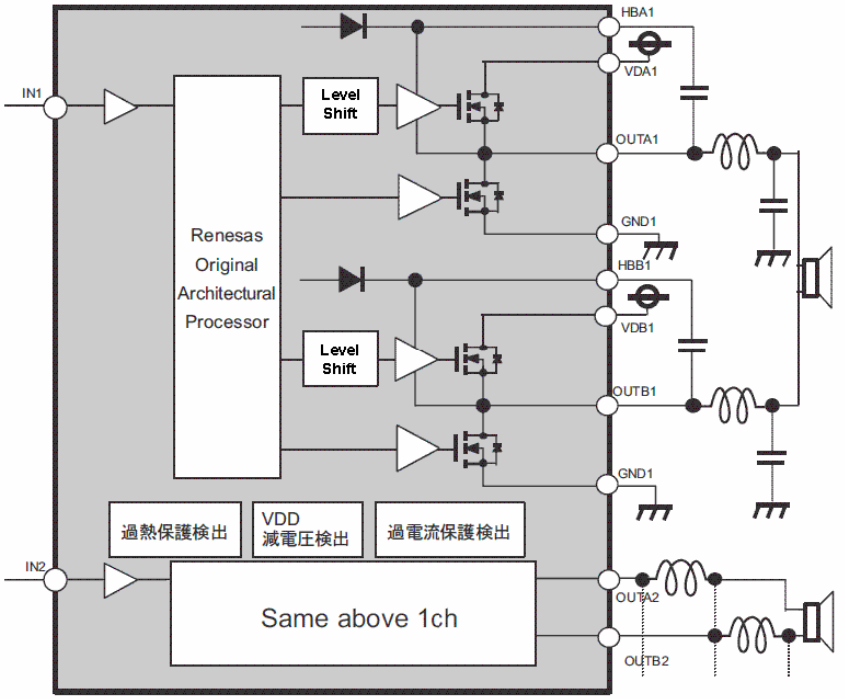
8.4. Digital Audio Amplifier.

In the WAX2 chassis a Digital Audio Amplifier M61571AFP is fitted on the AE board.
The left and right channel signals available at pins 27 and 28 of IC7001 (MSP4410K) are applied to the pins 8 and 19 of IC7007 (M61571AFP).
The outputs are pins 17,18, 41, 43 for the Left Speaker and the pins 31,32,36,38 for the Right Speaker.
This Audio Amplifier IC has also a STBY/MUTE input at pin 9 that is controlled by SP MUTE and LINE MUTE lines.

Audio out – Block diagram

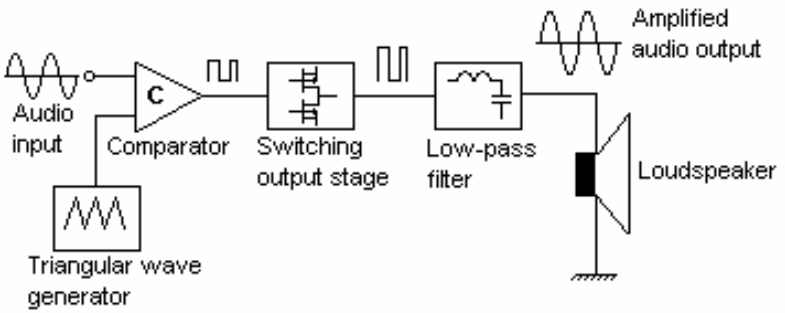


M61571AEP – Block diagram



8.4.1. Digital Audio Amplifier- basics

A Digital Audio Amplifier (or PWM) amplifier is a power amplifier where all active devices are operated in on/off mode. Output stages such as those used in pulse generators are examples of class D amplifiers. Mostly though, the term applies to devices intended to reproduce signals with a bandwidth well below the switching frequency. These amplifiers use mostly the pulse width modulation



The input signal is converted to a sequence of pulses whose averaged value is directly proportional to the amplitude of the signal at that time. The frequency of the pulses is typically ten or more times the highest frequency of interest in the input signal. The output of such an amplifier contains unwanted spectral components (i.e. the pulse frequency and its harmonics) that must be removed by a passive filter. The resulting filtered signal is then an amplified replica of the input.

A PWM (or Class-D) amplifier works on a similar principle as that of a switching power supplies (SMPS), except that the reference voltage of a PWM amplifier is the varying audio signal instead of a fixed voltage as in a SMPS. "PWM" stands for Pulse-width modulation.

The term "Class-D" is often misunderstood to mean "digital" amplifier. PWM or Class-D amplifiers are not digital amplifiers; the "D" is just a classification to differentiate it from other classes of amplifiers.

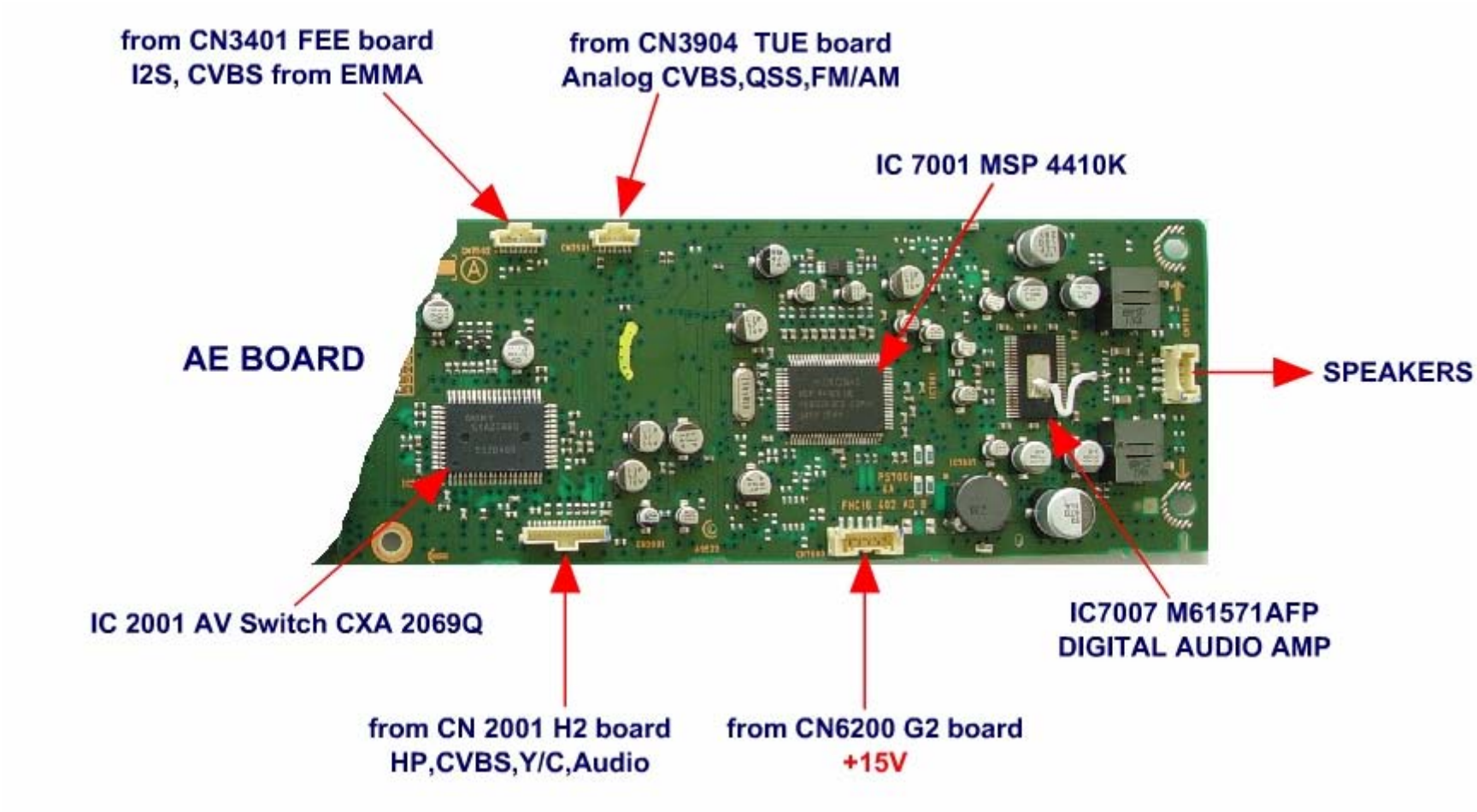
One way to create the PWM signal is to use a high speed comparator that compares a high frequency triangular wave and the audio input and generates a series of pulses such that the width of the pulses corresponds to the amplitude and frequency of the audio signal. The comparator then drives the output stage which is a high-power switch (usually comprised of MOSFETs) which generates a high-power replica of the comparator's PWM signal. This PWM output is fed to a low-pass filter which removes the high-frequency

switching components of the PWM signal to recover the audio information and feeds it to a loudspeaker. Use of a high enough switching frequency (or triangular waveform) is mandatory in order to obtain reasonably good frequency response and low distortion. Most class-D amplifiers use switching frequencies greater than 100 kHz. These high frequencies require most of the components in the amplifier to be capable of high speed operation. Another way to create the PWM signal is adopted when a SPDIF signal or other form of digital feed is available. The digital signal is fed to a DSP that uses software to create the PWM signal. The PWM signal is not usually fed directly to the MOSFETs but to some kind of MOSFET driver that can deliver the high currents required to make the MOSFETs work in the non-linear area (i.e., as switches rather than amplifiers).Usual problems encountered when designing class-D amps are, too short dead times and/or operation in the saturation area (for MOSFETs). Both the conditions typically results in catastrophic failure of the MOSFETs. The final frequency response and distortion depends not only on the switching frequency and the output filter but also on the load (or speaker system) connected to the amplifier's output. A speaker system may contain a single driver (loudspeaker) or multiple ones with a passive crossover. Loudspeaker impedance is not fixed and changes with audio frequency and this compounds with the passive crossover's own problems. This means that the load presented to the amplifier is not purely resistive and changes with the frequency of the audio signal that the amplifier outputs, thereby causing anomalies in the final frequency response (including peaking, oscillation and distortion). Hence many high-end class-D amplifiers employ negative feedback to correct for phase/frequency anomalies due to speaker impedance and the crossover. This makes the design of a class-D amplifier even more complex. But inspite of the complexity involved, a properly designed class-D amplifier offers the following benefits:

- Reduction in size and weight,
- Reduced power dissipation (heat) and hence smaller (or no) heatsinks,
- Reduction in cost due to smaller heat sink and compact circuitry,
- Very high power conversion (efficiency), usually ≥ 90%.

The high efficiency of a class-D amplifier stems from the fact that the switching output stage is never operated in the active (or linear for bipolar junction transistors) region. Instead, the output devices are either ON or OFF - both states representing minimum power dissipation in the output devices. When the devices are ON, the current through them is maximum but the voltage across the devices is (theoretically) zero and when the devices are OFF, the voltage across the devices is maximum but the current is zero. In both cases, the power dissipated ($V \times I$) is zero. This still leaves the signal with a great amount of energy in the form of harmonics, which must be filtered out. To maintain a high efficiency, the filtering is done with purely reactive components (inductors and capacitors), which store the excess energy until it is needed instead of converting it into heat.

8.5. AE BOARD – AUDIO PART



9. SYSTEM CONTROL

9.1. Micro Processor and I2C Bus structure.

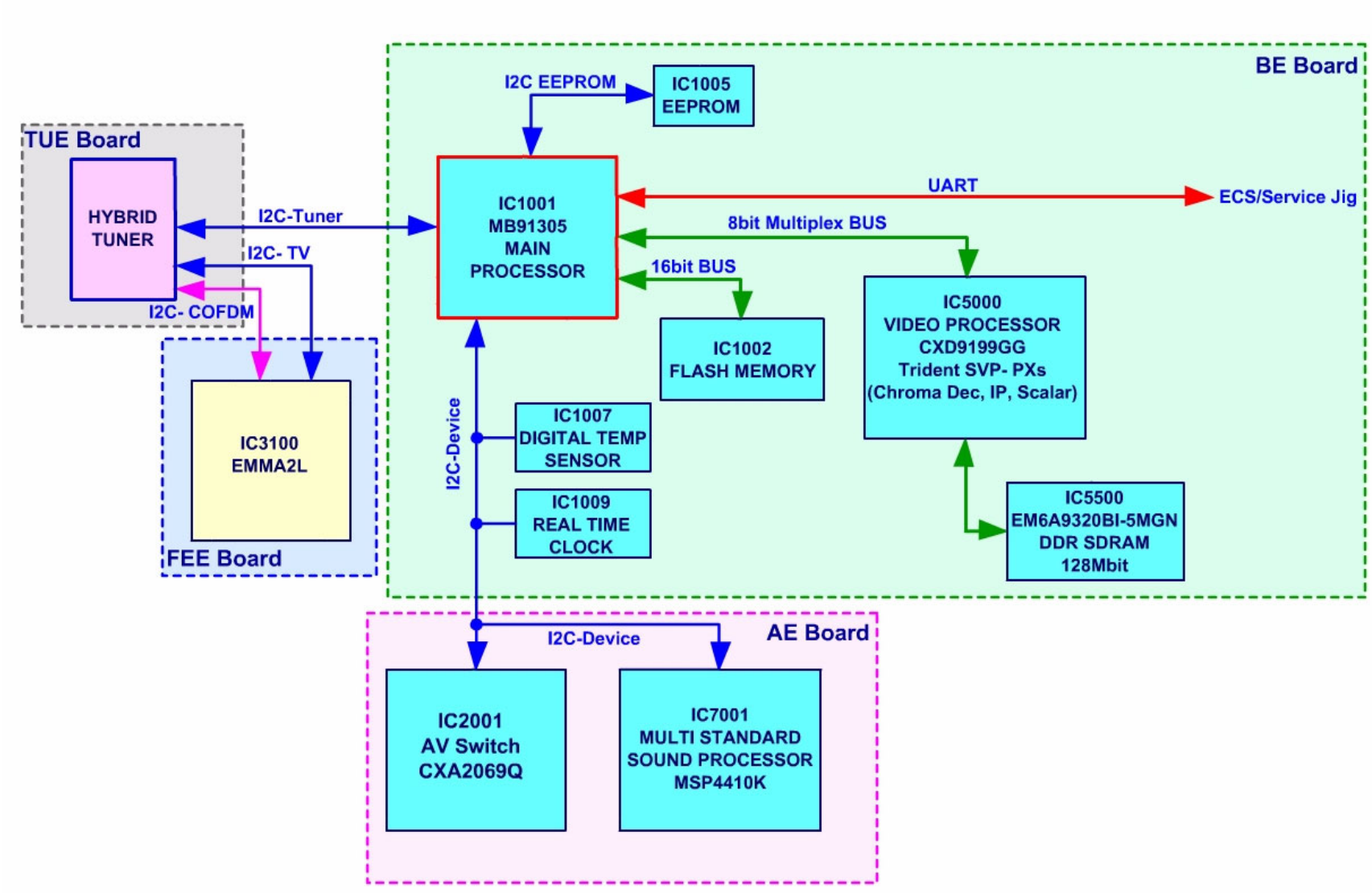
A new 32 Bit Micro Processor type MB91305 PMC from FUJITSU is used in the WAX 2 chassis.
The MB91305 Processor bases on a 32-bit RISC CPU core (FR family) that is offering a variety of I/O resources

The MB91305 PMC is the main processor in WAX 2 chassis. It controls all other devices using different communication methods.

- For the communication with Flash Memory (where the software is stored) a 16bit Bus is used.
- Communication with the Video Processor is accomplished using 8bit Multiplex Bus.
- Different, separated I2C Buses are used in order to communicate with simple devices. For instance, ICs on the AE board such as AV switch, MSP and IC1007 Digital Temp Sensor or the IC1009 RCT are connected to the Micro Processor via I2C- DEVICE BUS.
- Tuner and EMMA 2L use the I2C TUNER BUS. (Additional I2C COFDM bus connects Hybrid tuner with the EMMA processor)
- IC1005 NVM EEPROM uses own separated I2C EEPROM Bus.

- A special interface UART is used for the communication between the Micro Processor and the Service Connector.

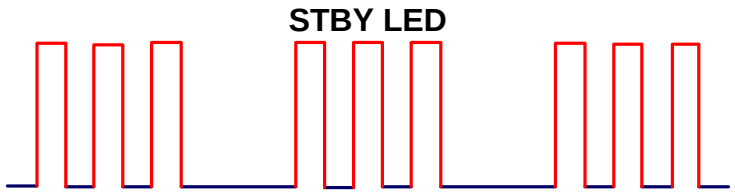
9.2. I2C BUS MAP



9.3. Self Diagnostic Software

The identification of errors within the WAX2 chassis is triggered in one of two ways: - 1: Busy or 2: Device failure to respond to IIC. In the event of one of these situations arising the software will first try to release the bus if busy (Failure to do so will report with a continuous flashing LED) and then communicate with each device in turn to establish if a device is faulty. If a device is found to be faulty the relevant device number will be displayed through the LED (Series of flashes which must be counted).

Flash Timing Example: e.g. error number 3

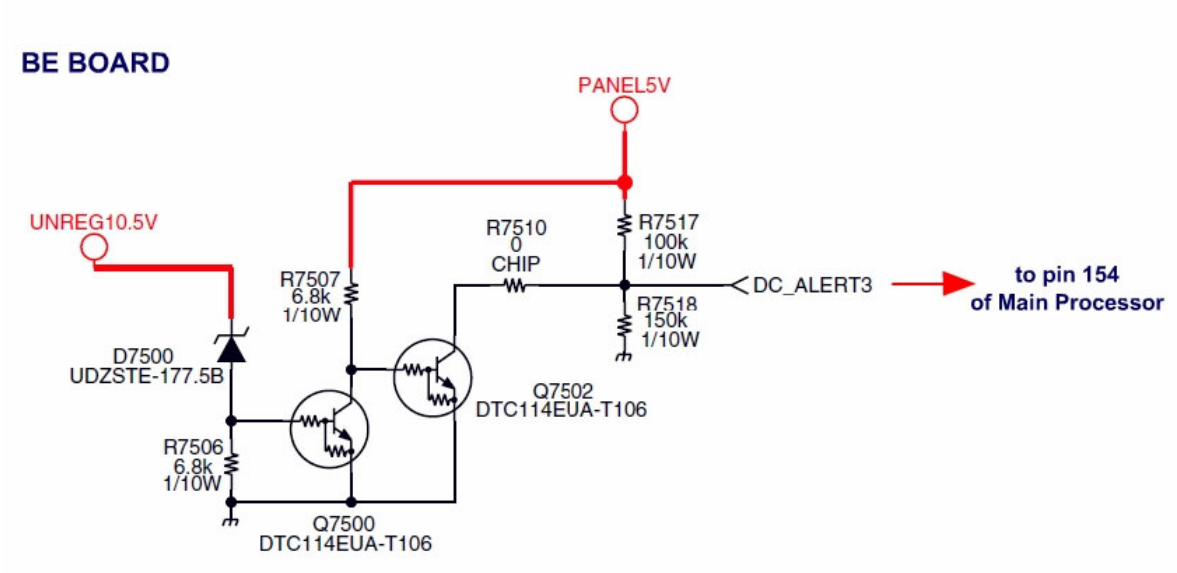


LED ERROR CODE	ERROR DESCRIPTION
1	UNREG33V Supply Voltage Trouble (DCALERT3)
2	VD1.8, DE5V/6V Voltage Trouble (DCALERT2)
3	UNREG10.5V, PANEL5V Voltage Trouble (DCALERT1)
4	Backlight Trouble
5	Main Supply Voltage Trouble
6	Speaker Applied Voltage Trouble
7	Monitor an Increase in Inside-Temperature (esp. on the panel side)
8	Trident IC Trouble
9	DTT Trouble (Communications / BS_CS_PROT)

9.4. Circuits supporting the SELF DIAGNOSTIC SOFTWARE

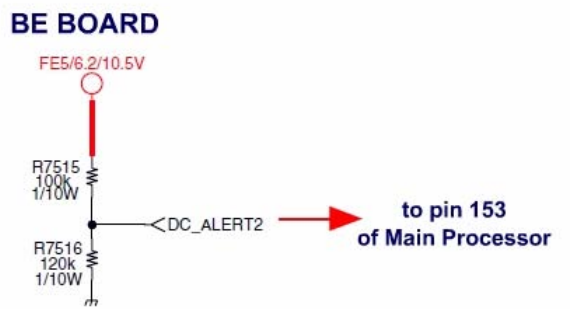
9.4.1. LED ERROR CODE 1

This circuit monitors the power voltage value of a panel (PANEL5V)
and a voltage value of Audio AMP (UNREG10.5V)



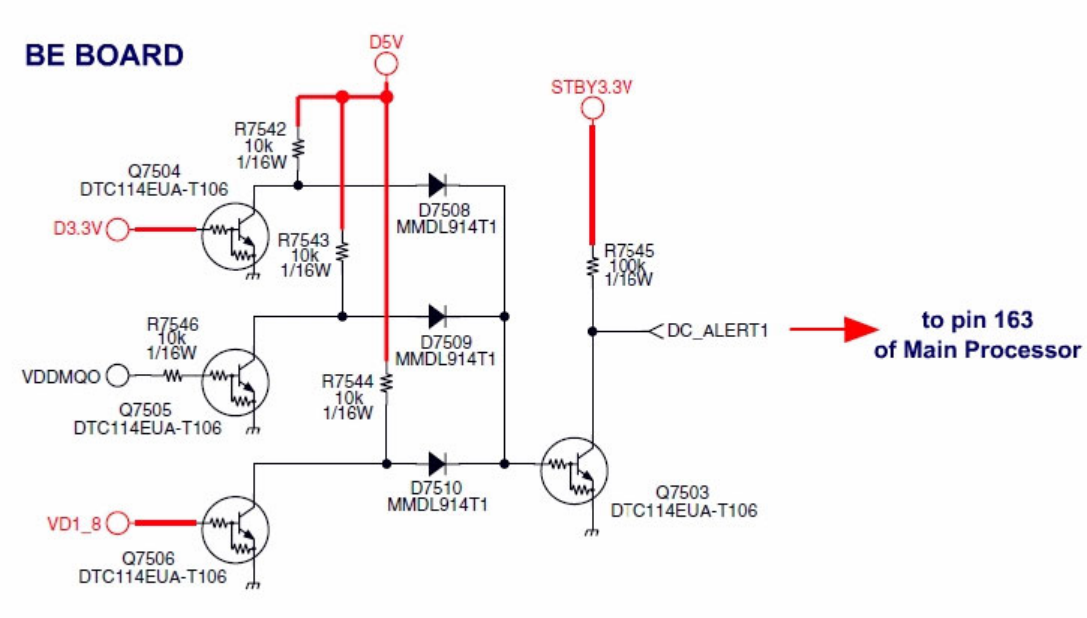
9.4.2. LED ERROR CODE 2

This circuit monitors the power voltage value
of a digital FE module FE5V (FE6V)



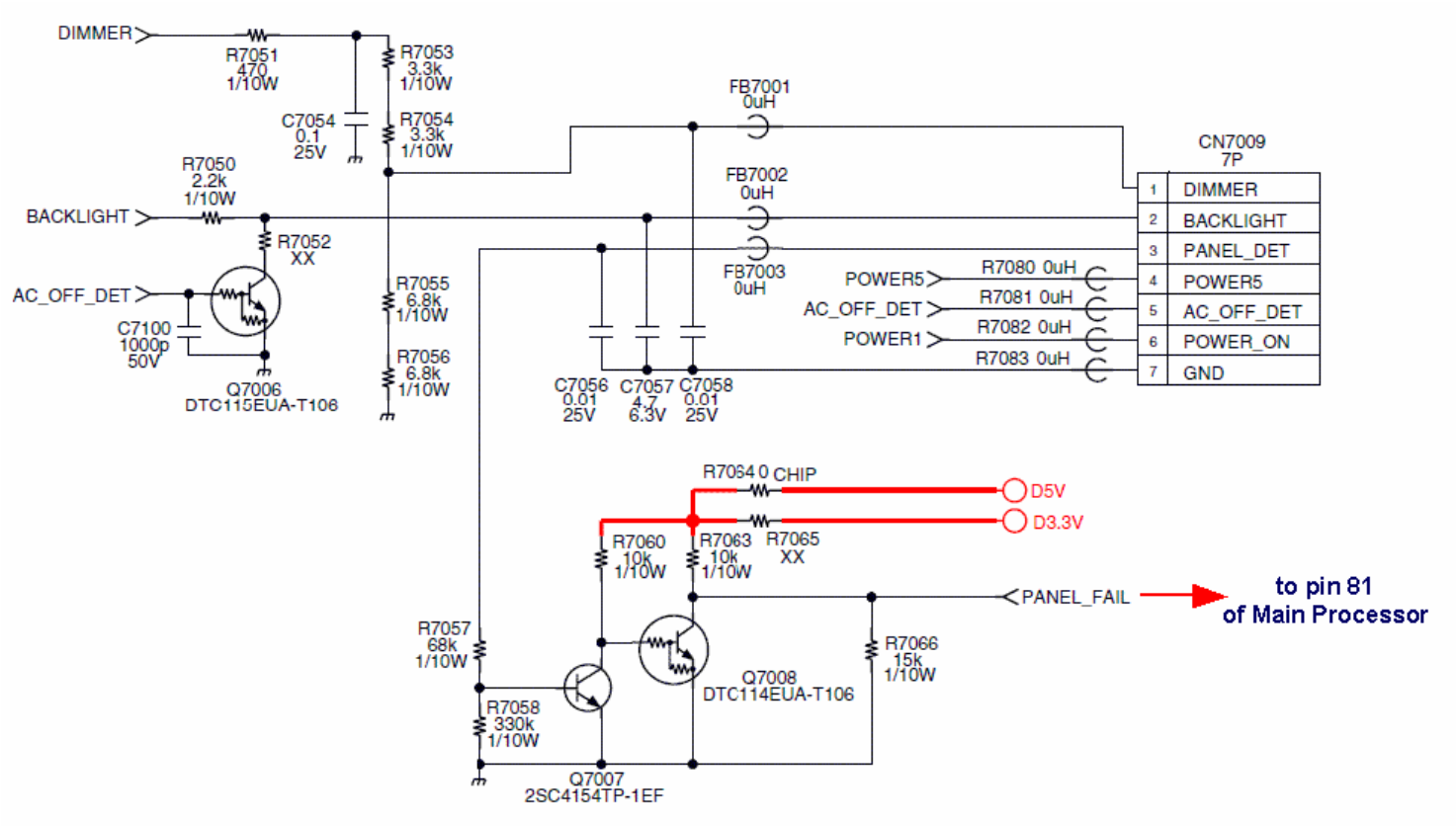
9.4.3. LED ERROR CODE 3

This circuit monitors the power voltage value of Trident (D3.3V/D2.5V/D1.8V).



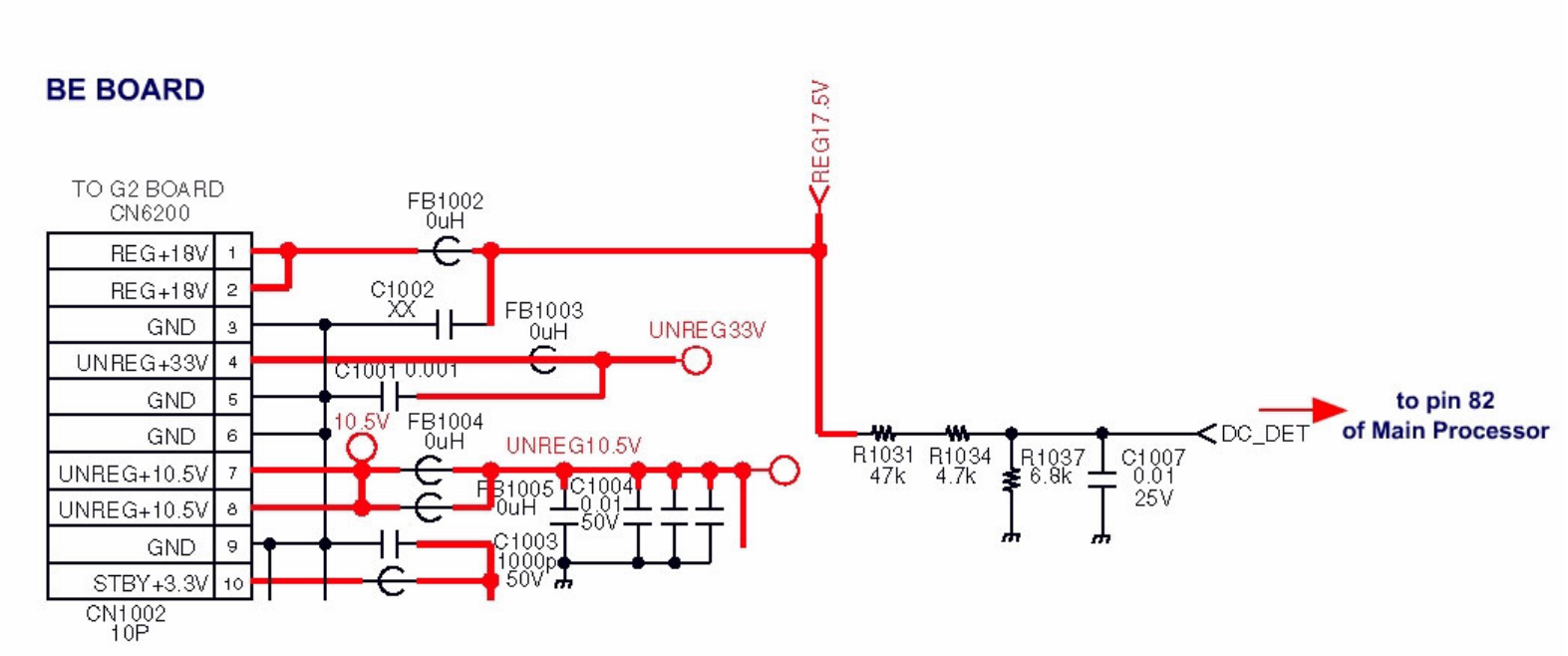
9.4.4. LED ERROR CODE 4

This circuit monitors an inverter's operational trouble and an increase of current (PANEL_DET (FAIL))



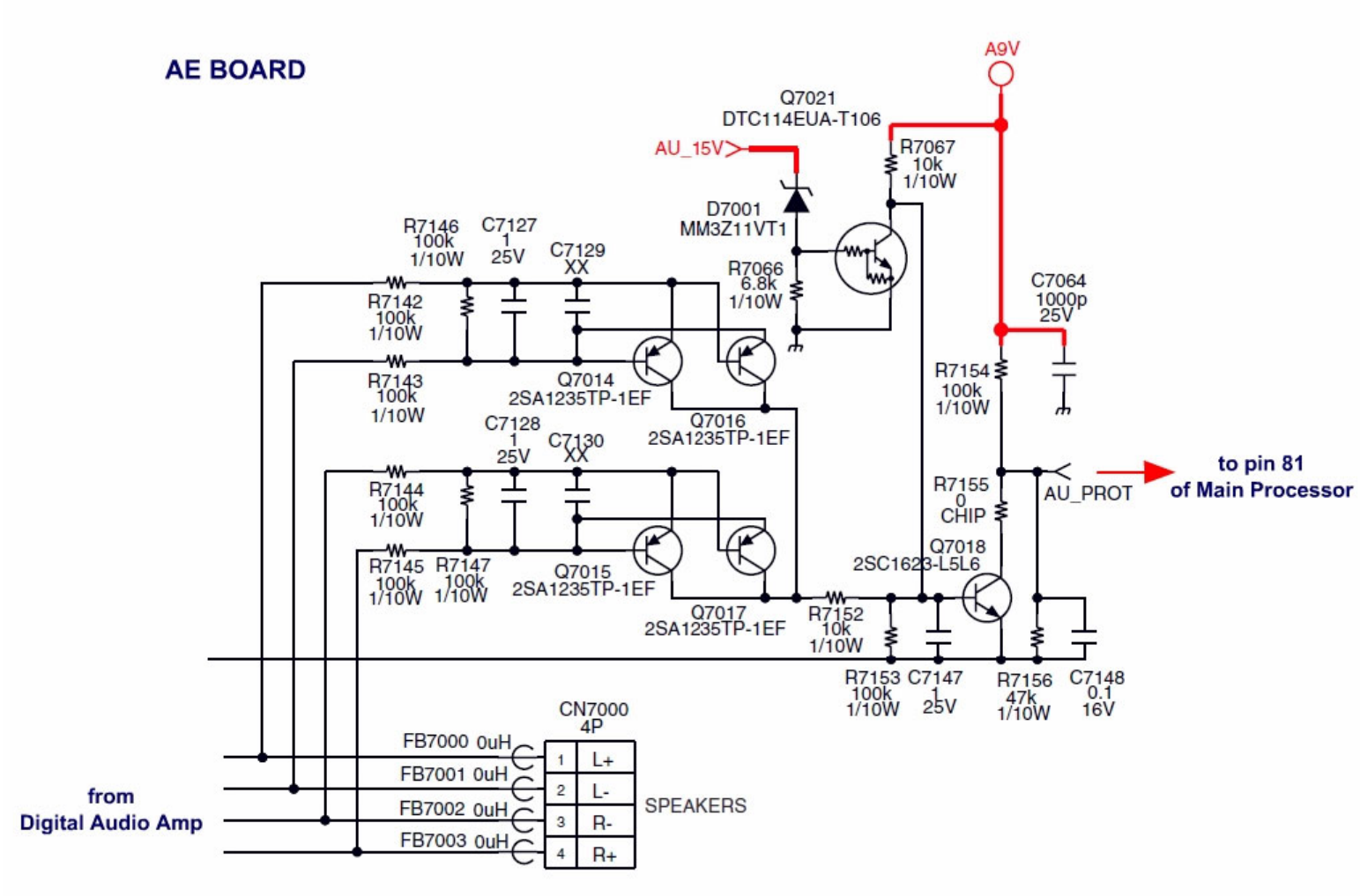
9.4.5. LED ERROR CODE 5

This circuit monitors the value of voltage of a main supply line (17.5V_DET).



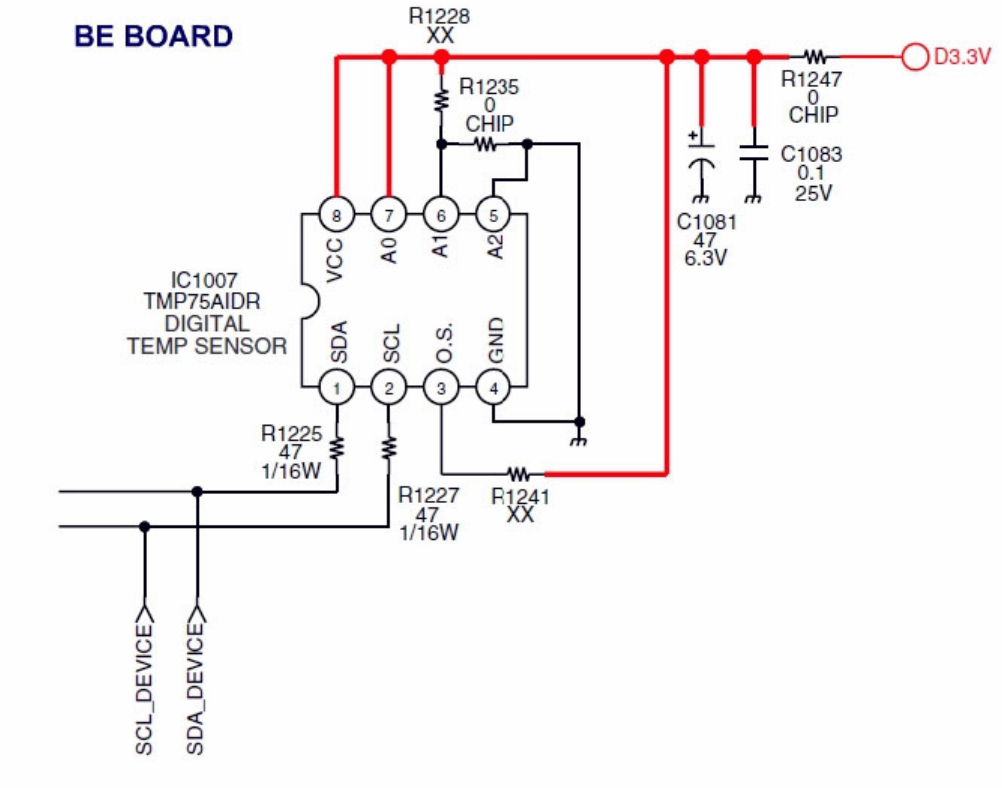
9.4.6. LED ERROR CODE 6

This circuit monitors a trouble of DC application to speakers (AU_PROT).



9.4.7. LED ERROR CODE 7

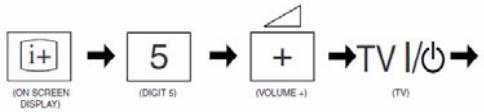
This circuit monitor an increase of inside-temperature.



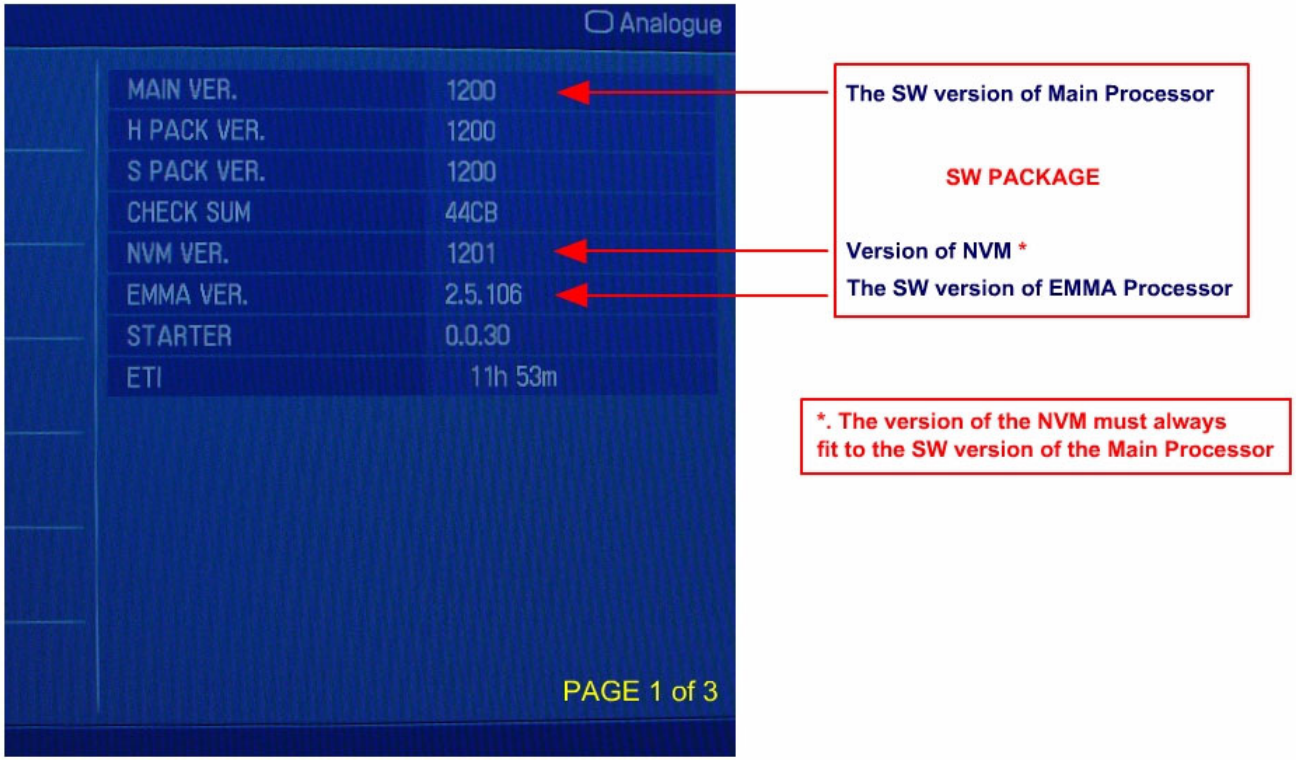
9.5. Service Mode

Service adjustments to this model can be performed using the supplied remote Commander RM-ED005.
How to enter into Service Mode?

- Switch the TV set to **„Standby „**condition
- Press the following sequence of buttons on the Remote Commander.

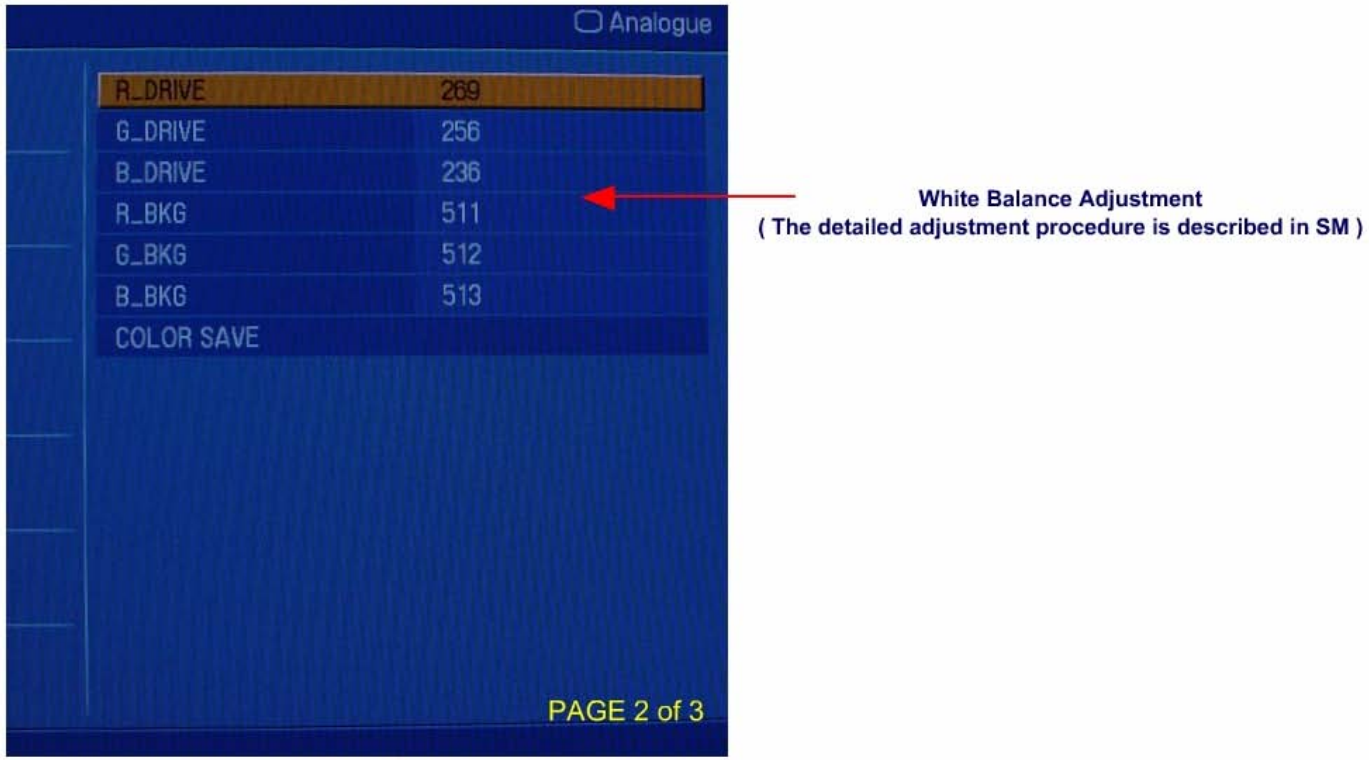


- Push "MENU" key on the remote commander and the following menu will then appear on the screen.
  (WAX 2 chassis has a very simple service mode – only 3 pages are available)



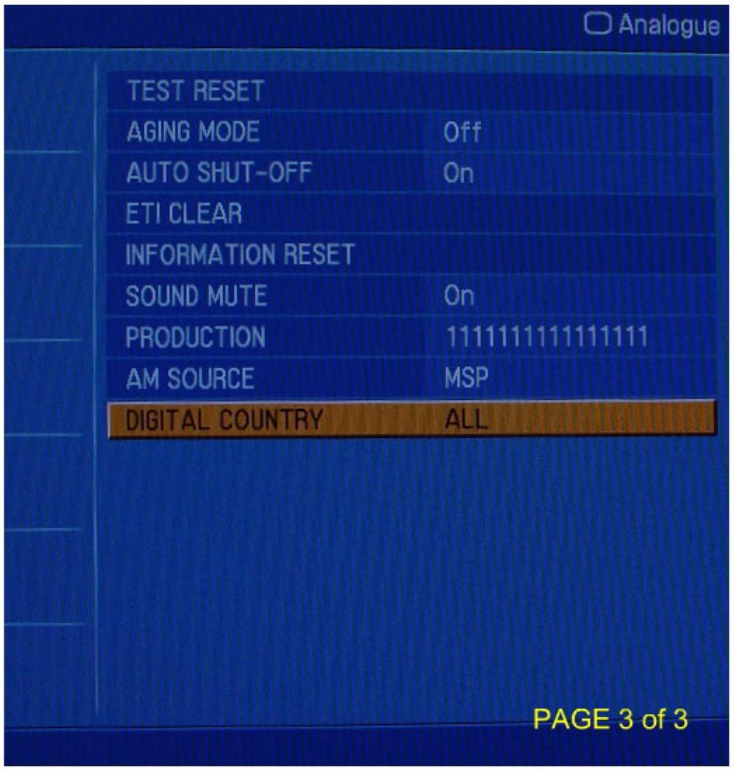
White Balance Adjustment

It is the only one adjustment that can be done using the Service Mode



The Signal Level Adjustment can be performed using the TL 3.

The page 3 of the service mode displays several factory settings. Some of them can be used in service as well e.g. ETI Clear



In order to leave the “Service Menu” switch the TV set OFF and then ON.

9.6. Data handling and Software update.

The NVM data handling and the software update procedure is very similar to procedure used in already known AT2X chassis.
In order to read/write the NVM data that is stored in the IC1005 EEPROM on the BE board we need an interface board (TL3 Jig) and a **CODE 2 application for WAX2 chassis**
(Please note that the CODE 2 software used for AT2X doesn't communicate with WAX2)

In the WAX 2 chassis are two kind of software are available (the versions of the software can be checked in Service Menu)

1. Main Processor software: It is stored in the IC 1002 Flash Memory on the BE board
   The update of the Main Processor software is done using the TL3 Jig and the Flash Memory Programmer application from Fujitsu (FR-Fujitsu).

2. Emma Processor software: This software is stored in the IC 3206 Flash Memory on the FEE board.
   The software upgrade can be done **Over-The-Air** (if this kind of service is available) or using Memory Stick (a hidden Memory Stick slot is available on the FEE board)

IMPORTANT NOTES!

- Please be informed that all applications and software files required for the Data Handling and the Software Update will be available for authorized service stations via ASSIST

- The Software and NVM files are provided in Packages.
  Please make sure that the NVM and SW files which you are using for the updates belong to the same Software Package

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